

VBLE4 / VBLE5

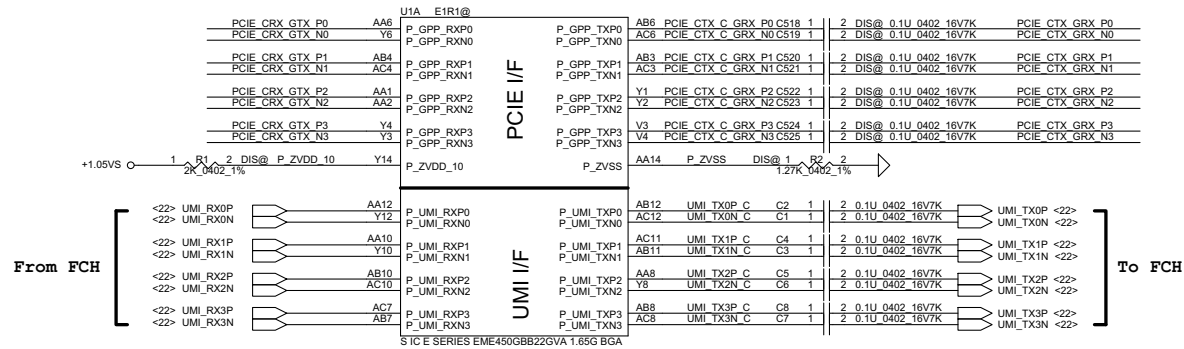
Eureka

LA-8868P REV 1.0 Schematic

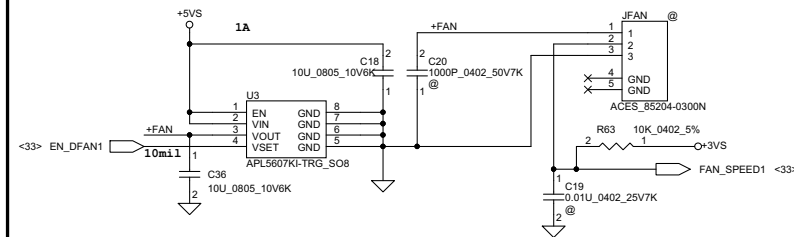
**AMD Brazos 2.0 / Zacate APU / Hudson-M3L FCH
2012-07-12 Rev 1.0**

Security Classification	Compal Secret Data			Title	
Issued Date	2012/05/18	Deciphered Date	2013/10/05	SCHEMATIC, MB A8868	
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				4019K4	B
Date: Saturday, September 07, 2013				Sheet	1 of 47

<11> PCIE_CTX_GRX_P[3..0] ← PCIE_CTX_GRX_P[3..0]
 <11> PCIE_CTX_GRX_N[3..0] ← PCIE_CTX_GRX_N[3..0]
 <11> PCIE_CRX_GTX_P[3..0] ← PCIE_CRX_GTX_P[3..0]
 <11> PCIE_CRX_GTX_N[3..0] ← PCIE_CRX_GTX_N[3..0]



FAN Control Circuit



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				4019K4	
				Date: Saturday, September 07, 2013	Sheet 5 of 47

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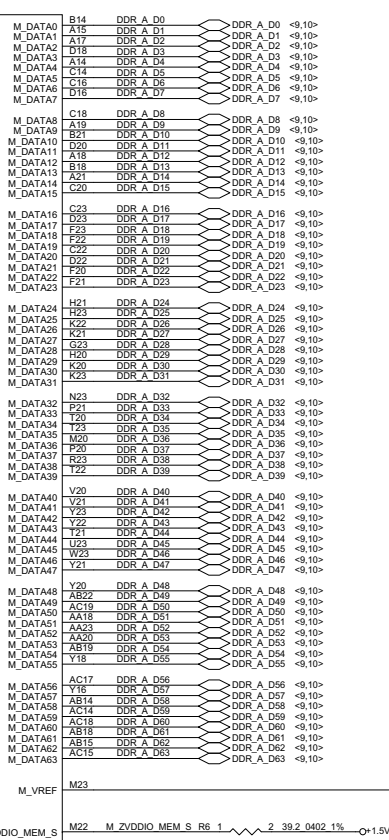
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Document Number 4019K4

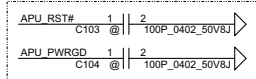
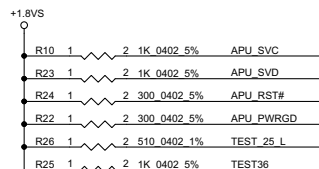
Date: Saturday, September 07, 2013 Sheet 5 of 47



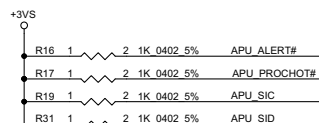
DDR SYSTEM MEMORY



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				4019K4	
				Date	Saturday, September 07, 2013
				Sheet	6 of 47



12/13 For debug if layout cross mote



TO EC

<18,33> EC_SMB_CK2

<18,33> EC_SMB_DA2

<22,33> H_PROCHOT#

<43> APU_VDDNB_RUN_FB_H

<43> APU_VDD0_RUN_FB_H

<43> APU_VDD0_RUN_FB_L

<43> APU_VDDNB_RUN_FB_L

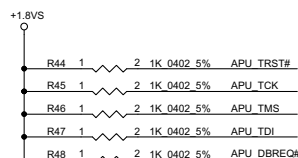
Check

<43> APU_VDD0_RUN_FB_L

<43> APU_VDDNB_RUN_FB_L

9/26 Add R931 R932 for AMD common design

AMD HDT Debug Conn



+1.8VS

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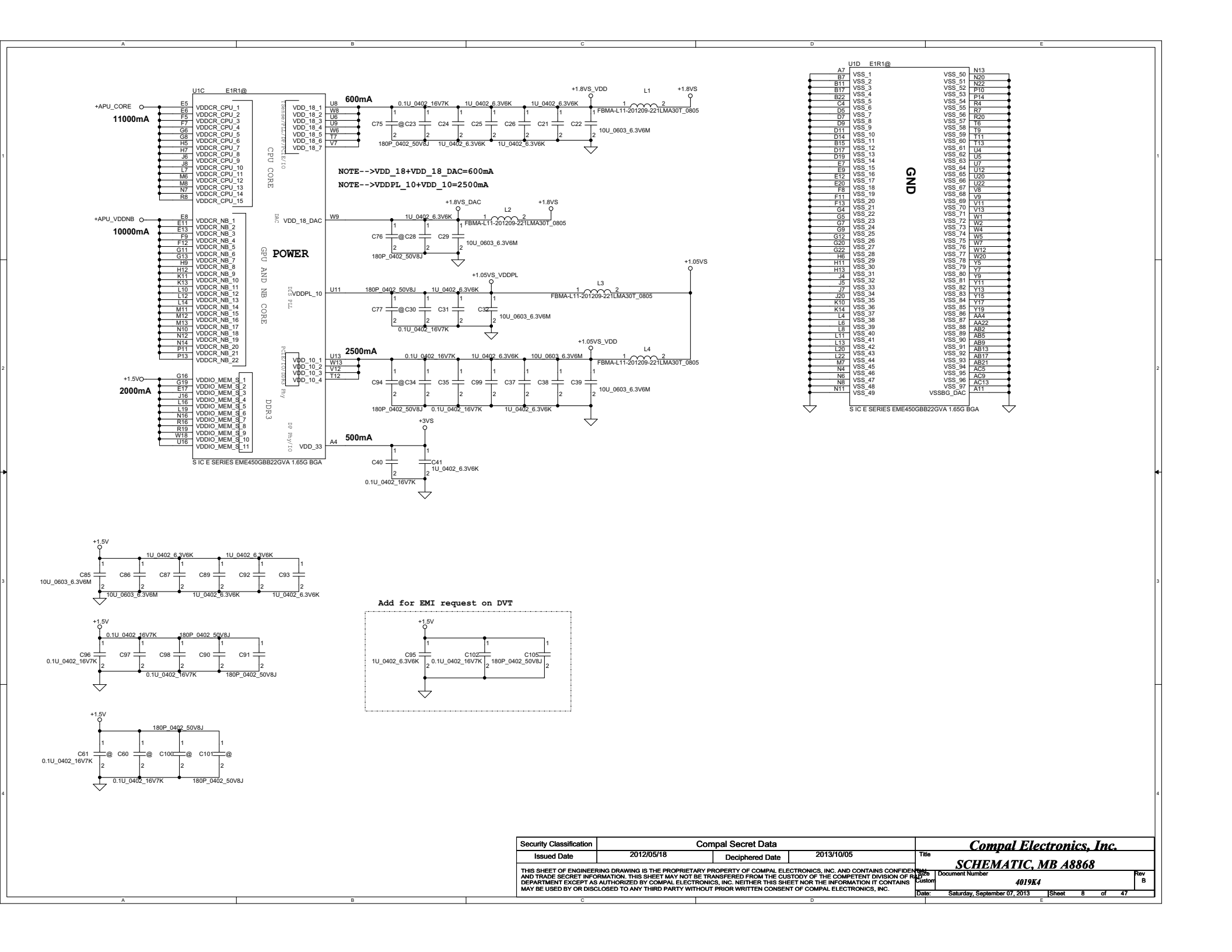
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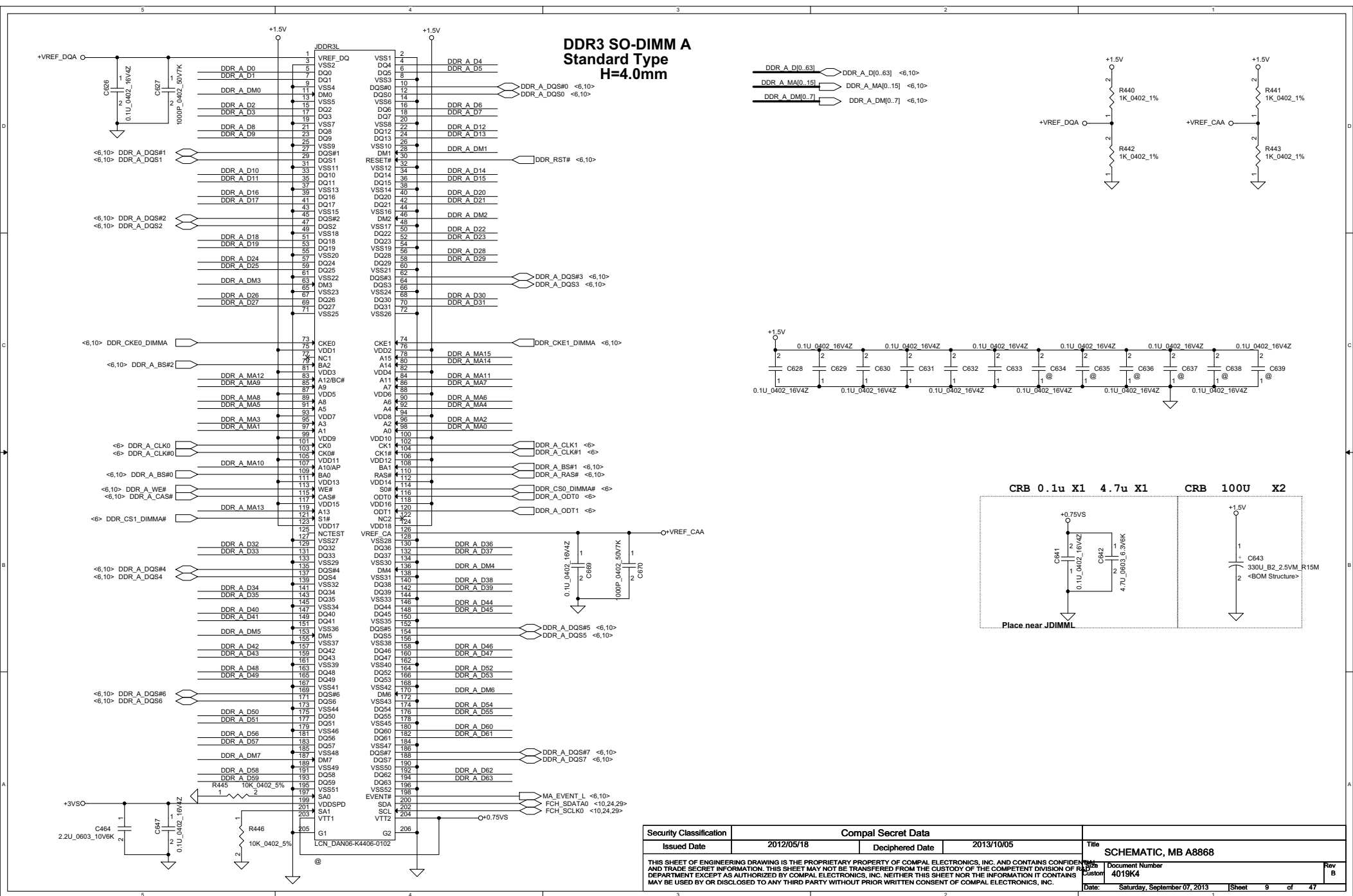
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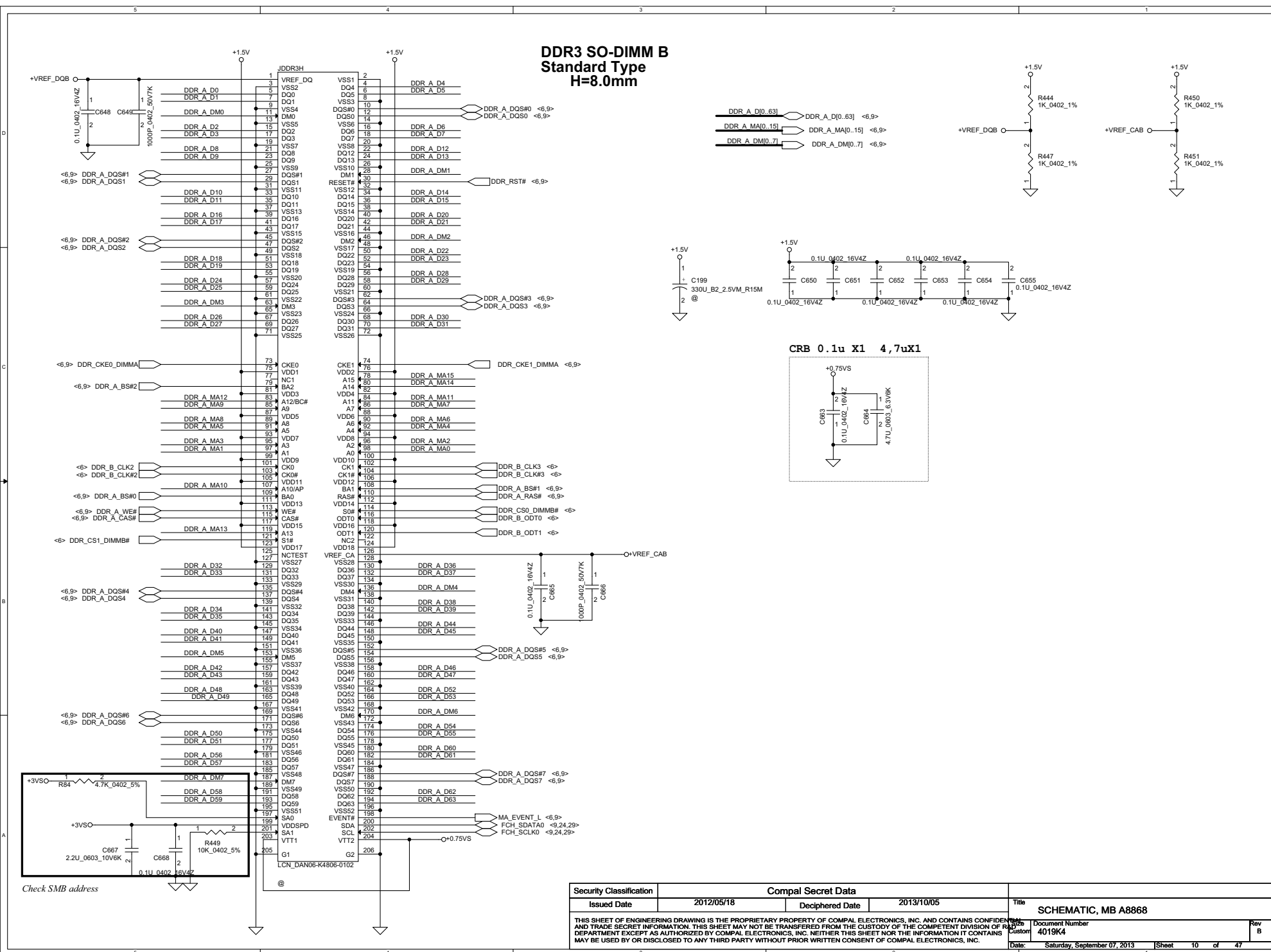
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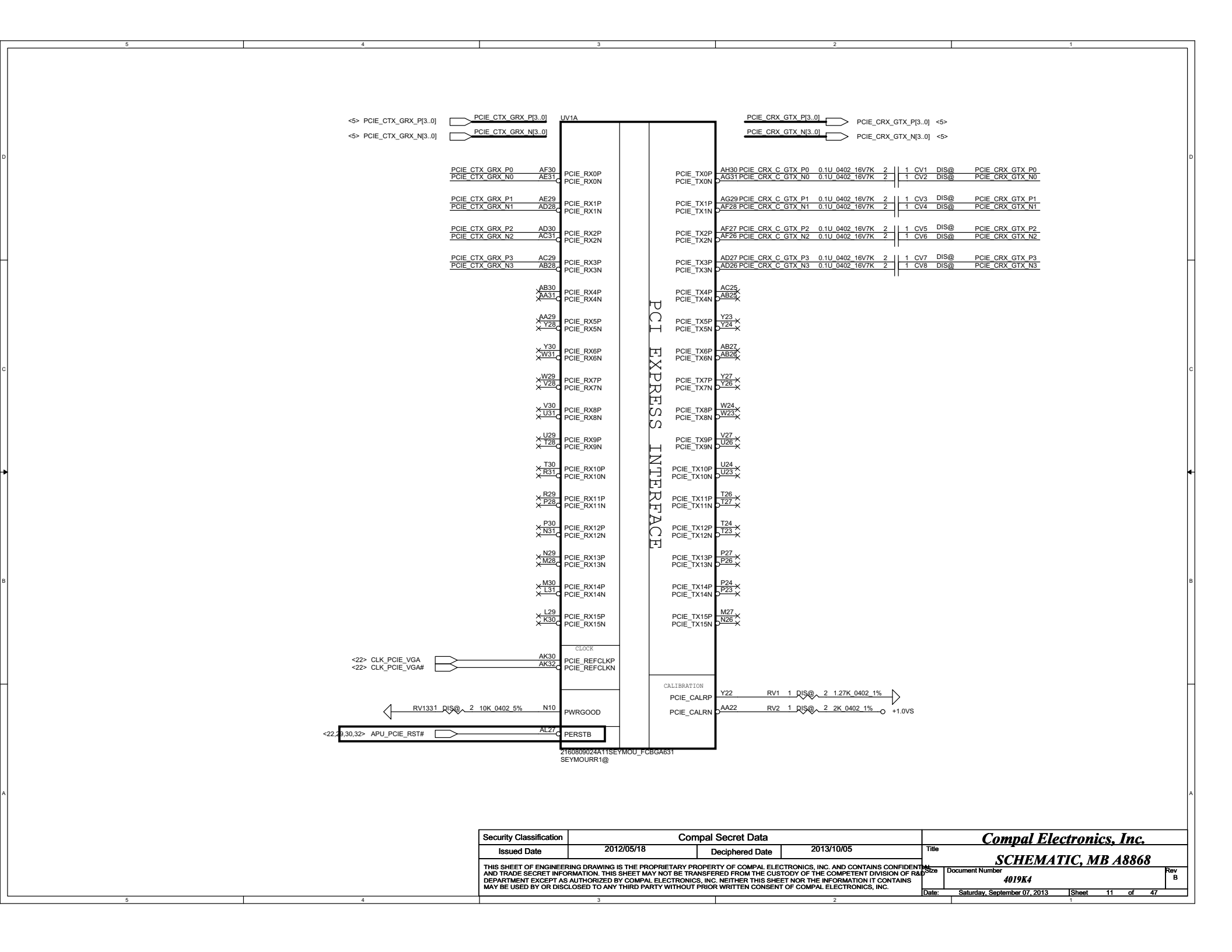
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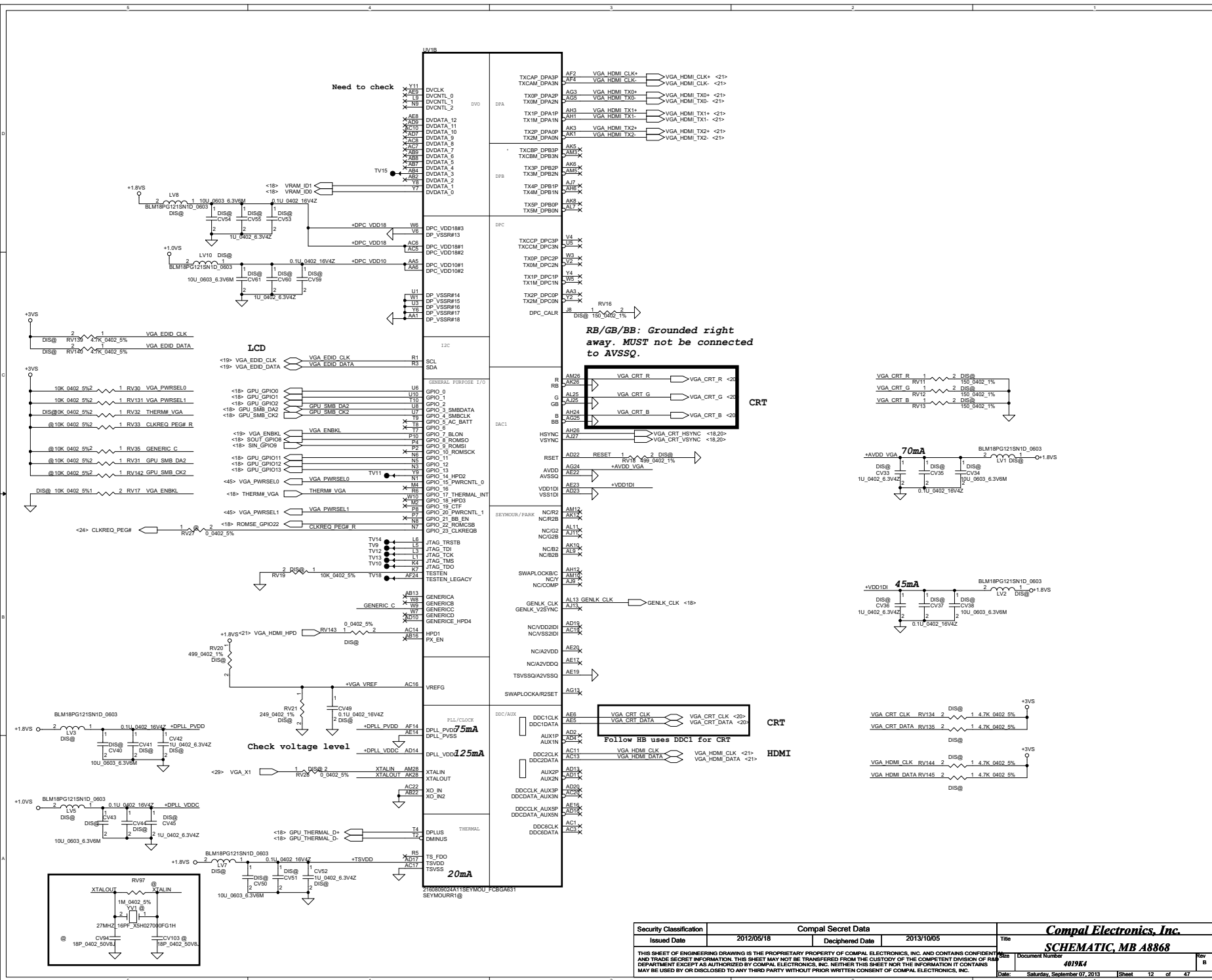


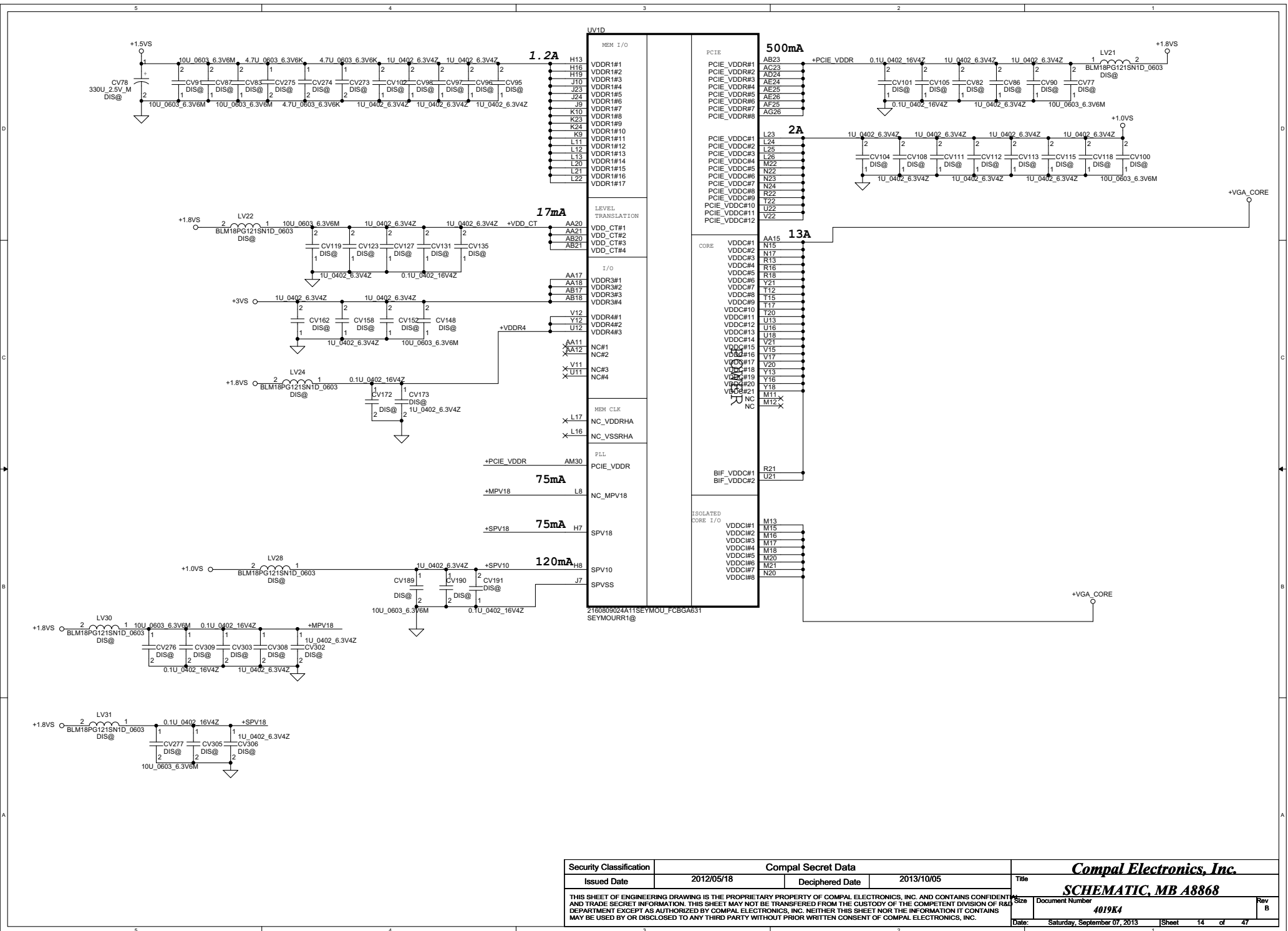




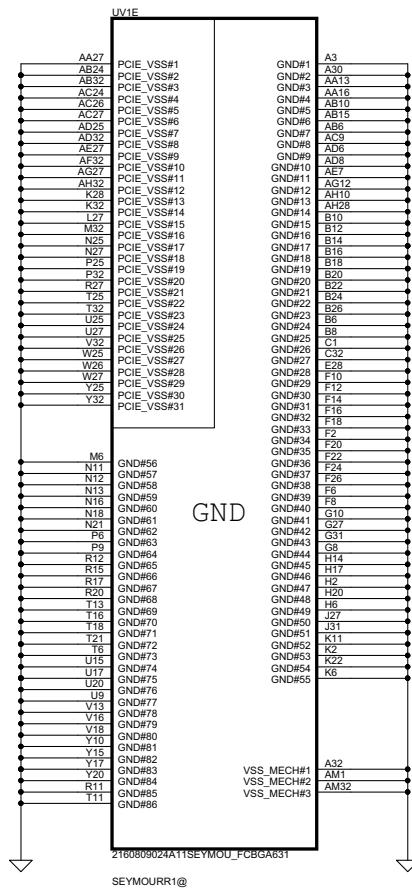


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				Date:	Saturday, September 07, 2013
				Sheet	11 of 47



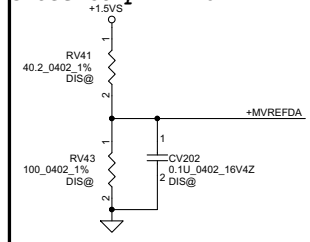


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				4019K4	Rev B
Date:				Saturday, September 07, 2013	Sheet 14 of 47

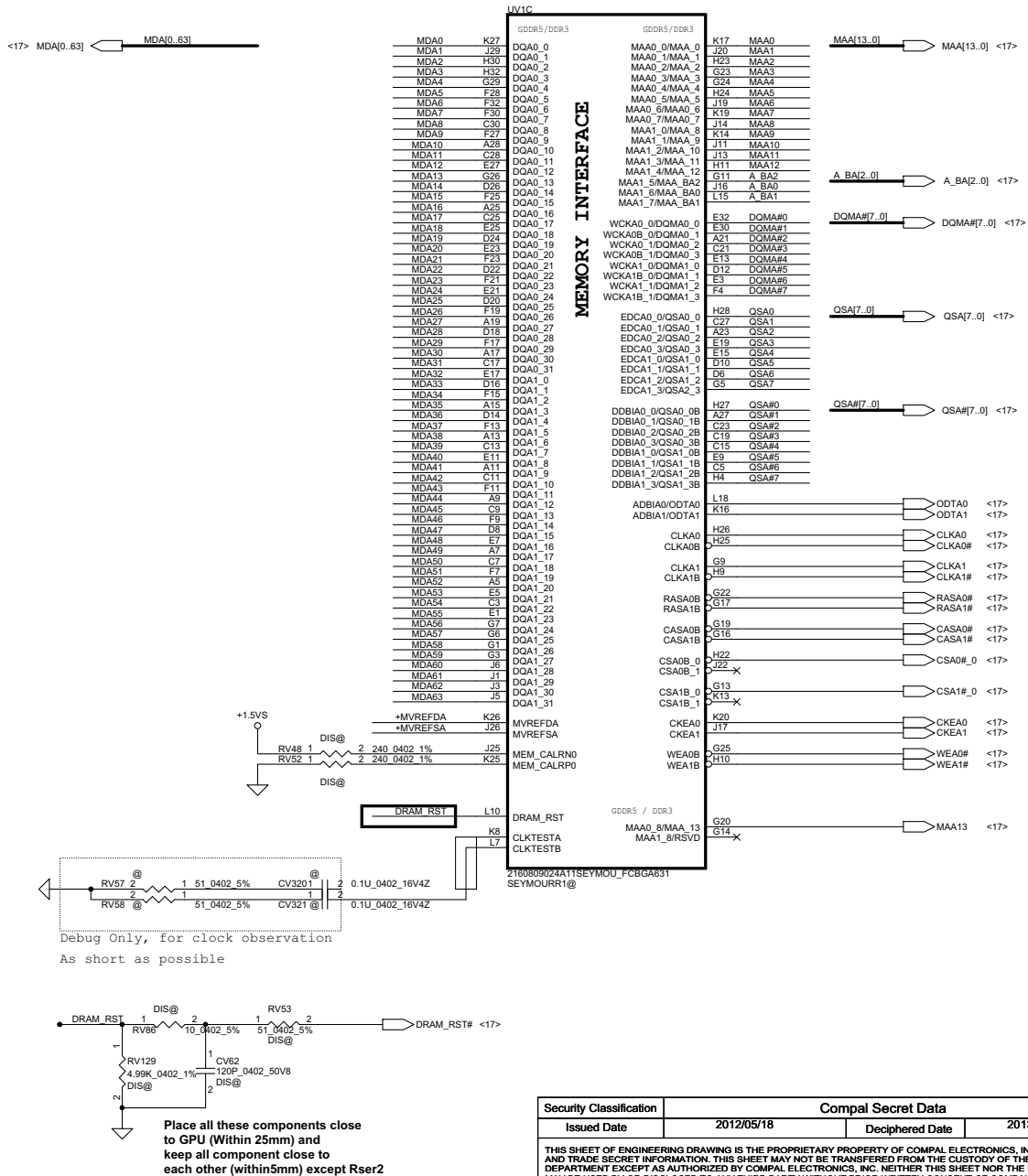
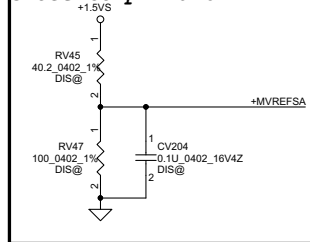


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				Date:	Saturday, September 07, 2013
				Sheet	15 of 47

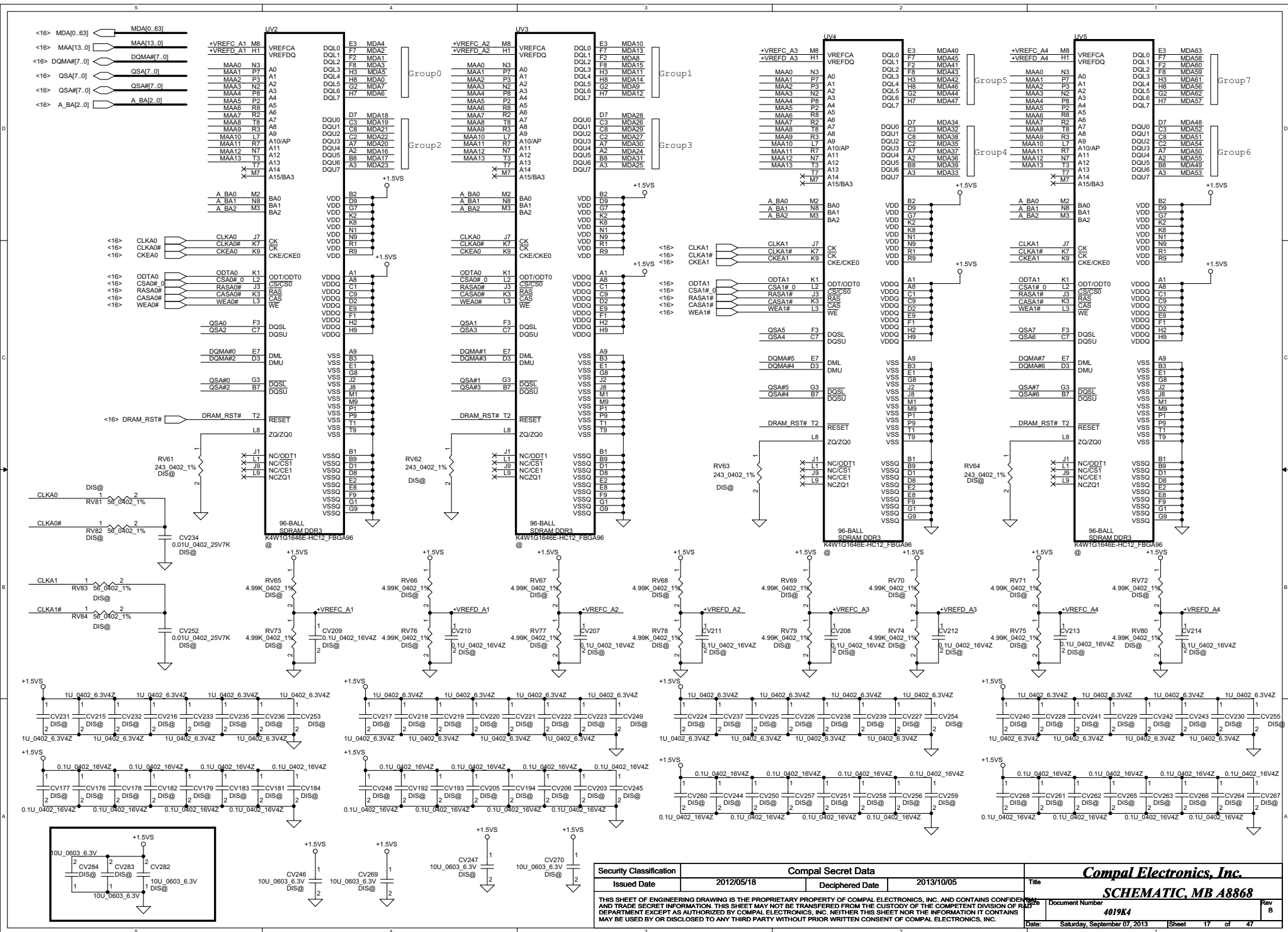
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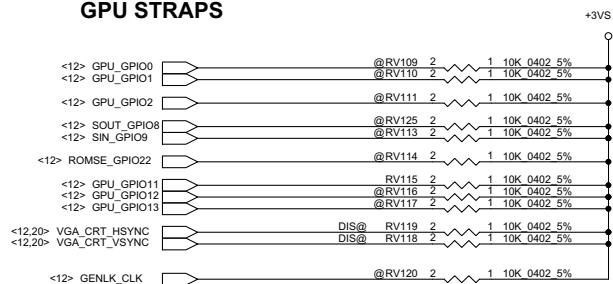
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				4019K4	
				Date: Saturday, September 07, 2013	Sheet 16 of 47

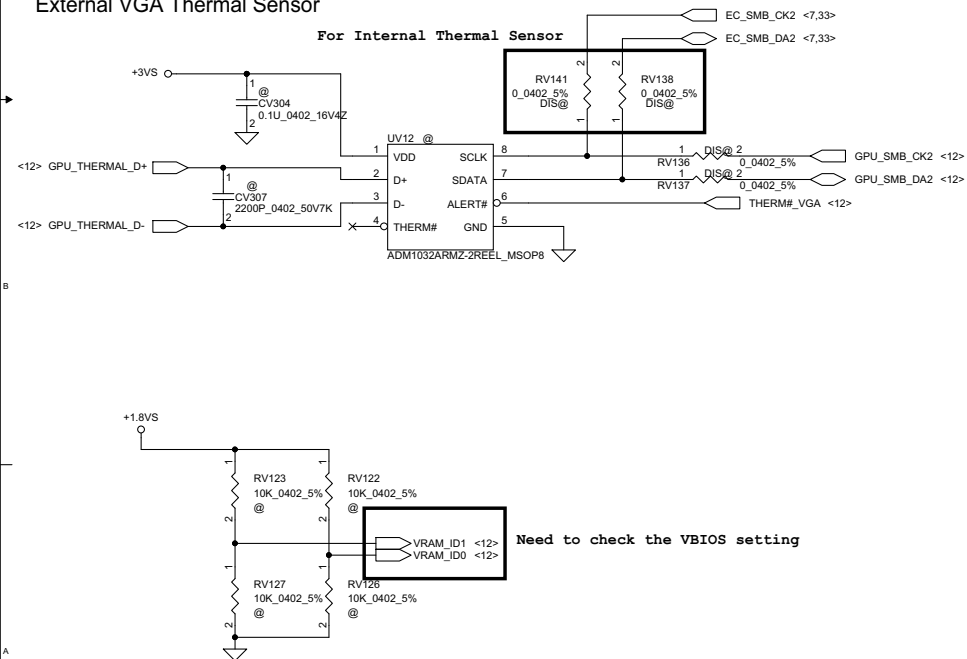


GPU STRAPS



GPU by the system BIOS		GPU by VBIOS
GPIO22 = 0 (BIOS_ROM_EN = 0)		GPIO22 = 1 (BIOS_ROM_EN = 1)
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]
0 0 0	128MB	1 0 0
0 0 1	256MB	(M25P05A)
0 1 0	64MB	

External VGA Thermal Sensor



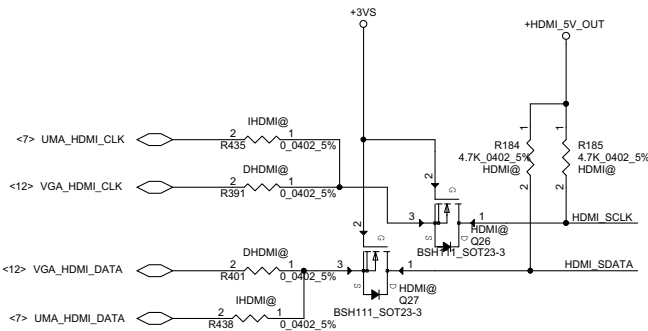
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

Straps Name	Pin Name	Net Name	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	GPU_GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	GPU_GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	0
BIF_GEN2_EN_A	GPIO2	GPU_GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0 5.0 GT/s capability will be controlled by software
RESERVED	GPIO_8_ROMSO	SOUT_GPIO8	RESERVED	0
RESERVED	GPIO_21_BB_EN	N.C	RESERVED	0 (Internal pulldown)
VGA_DIS	GPIO_9_ROMSI	SIN_GPIO9	VGA Controller 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	ROMSE_GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
CONFIG(2:0)	GPIO[13:11]	GPU_GPIO11 GPU_GPIO12 GPU_GPIO13	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	0 0 1 (256M)
RESERVED	GENLK_CLK	GENLK_CLK		0
AUD[1] AUD[0]	HSYNC VSYNC	VGA_CRT_HSYNC VGA_CRT_VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	0 0

STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 1,0	
VRAM_ID[1:0]	DVDDATA (1,0)	Seymour-S3	512M 64Mx16 (x4)	SAM K4W1G1646G-BC11	SA00004GS00	1 0	
			1G 128Mx16 (x4)	SAM K4W2G1646C-HC11	SA000047Q00	1 1	

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Date: Saturday, September 07, 2013				Sheet: 18	of: 27

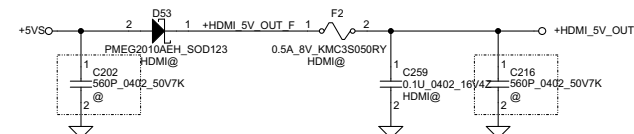
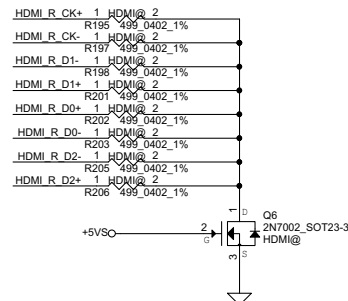
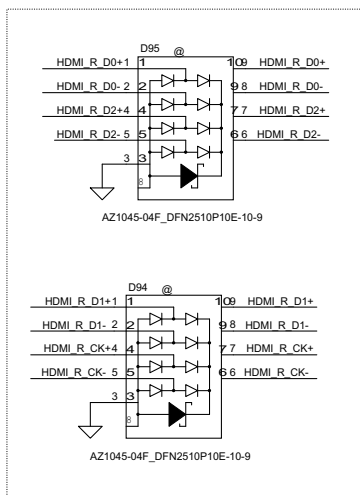
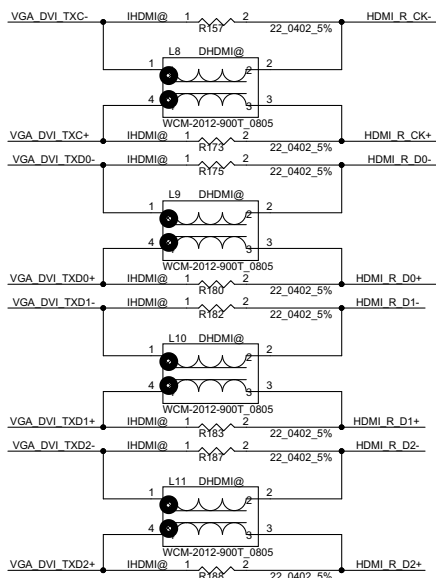
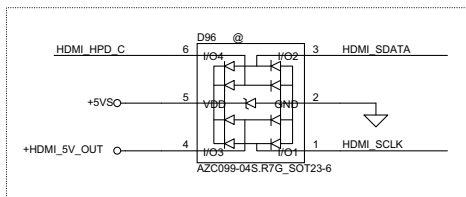


DISCRETE

<12> VGA_HDMI_CLK+	CV296	1	2	0.1U_0402_16V7K_DHDMI@	VGA_DVI_TXC+
<12> VGA_HDMI_CLK-	CV293	1	2	0.1U_0402_16V7K_DHDMI@	VGA_DVI_TXC-
<12> VGA_HDMI_TX0+	CV294	1	2	0.1U_0402_16V7K_DHDMI@	VGA_DVI_TXD0+
<12> VGA_HDMI_TX0-	CV297	1	2	0.1U_0402_16V7K_DHDMI@	VGA_DVI_TXD0-
<12> VGA_HDMI_TX1+	CV299	1	2	0.1U_0402_16V7K_DHDMI@	VGA_DVI_TXD1+
<12> VGA_HDMI_TX1-	CV298	1	2	0.1U_0402_16V7K_DHDMI@	VGA_DVI_TXD1-
<12> VGA_HDMI_TX2+	CV295	1	2	0.1U_0402_16V7K_DHDMI@	VGA_DVI_TXD2+
<12> VGA_HDMI_TX2-	CV300	1	2	0.1U_0402_16V7K_DHDMI@	VGA_DVI_TXD2-

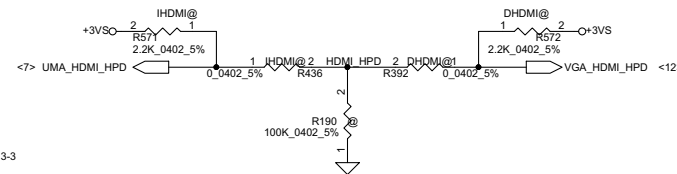
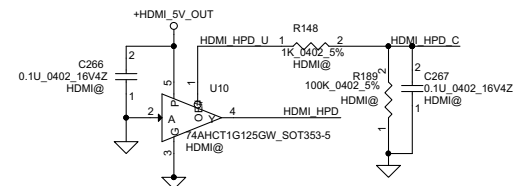
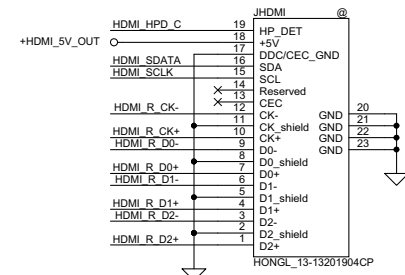
UMA

<7> UMA_HDMI_TXC+	C838	1	2	0.1U_0402_16V7K_IHDMI@	VGA_DVI_TXC+
<7> UMA_HDMI_TXC-	C837	1	2	0.1U_0402_16V7K_IHDMI@	VGA_DVI_TXC-
<7> UMA_HDMI_TX0+	C843	1	2	0.1U_0402_16V7K_IHDMI@	VGA_DVI_TXD0+
<7> UMA_HDMI_TX0-	C844	1	2	0.1U_0402_16V7K_IHDMI@	VGA_DVI_TXD0-
<7> UMA_HDMI_TX1+	C841	1	2	0.1U_0402_16V7K_IHDMI@	VGA_DVI_TXD1+
<7> UMA_HDMI_TX1-	C842	1	2	0.1U_0402_16V7K_IHDMI@	VGA_DVI_TXD1-
<7> UMA_HDMI_TX2+	C839	1	2	0.1U_0402_16V7K_IHDMI@	VGA_DVI_TXD2+
<7> UMA_HDMI_TX2-	C840	1	2	0.1U_0402_16V7K_IHDMI@	VGA_DVI_TXD2-



4/23 Add C202 and C216 for EMI request

HDMI Connector

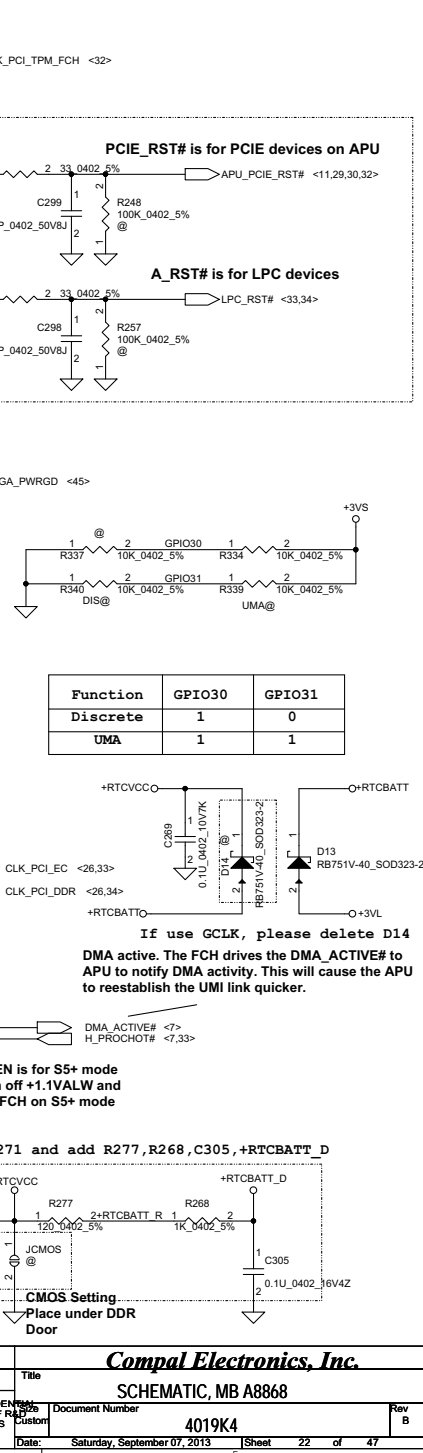


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Date:		Saturday, September 07, 2013		Sheet	21 of 47

Reserve ESD for HDMI conn. on DVT

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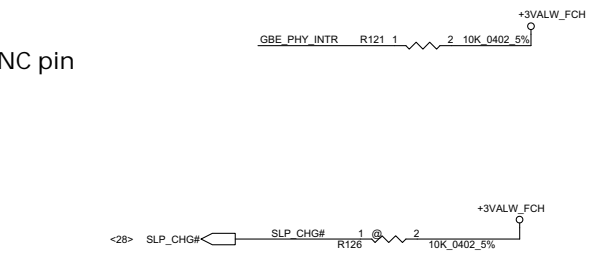
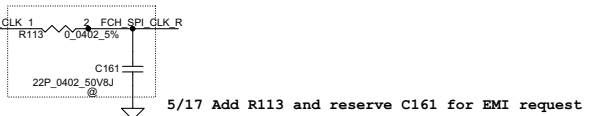
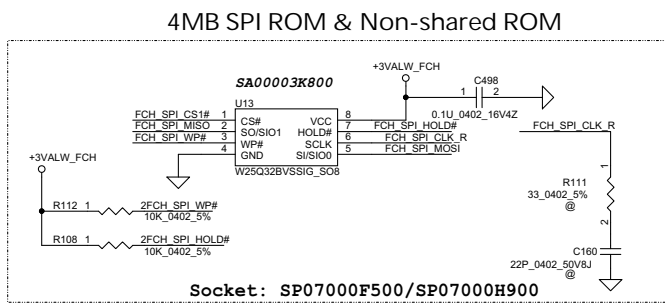
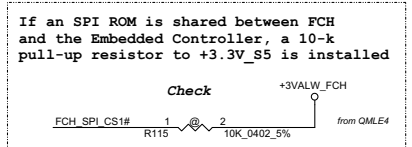
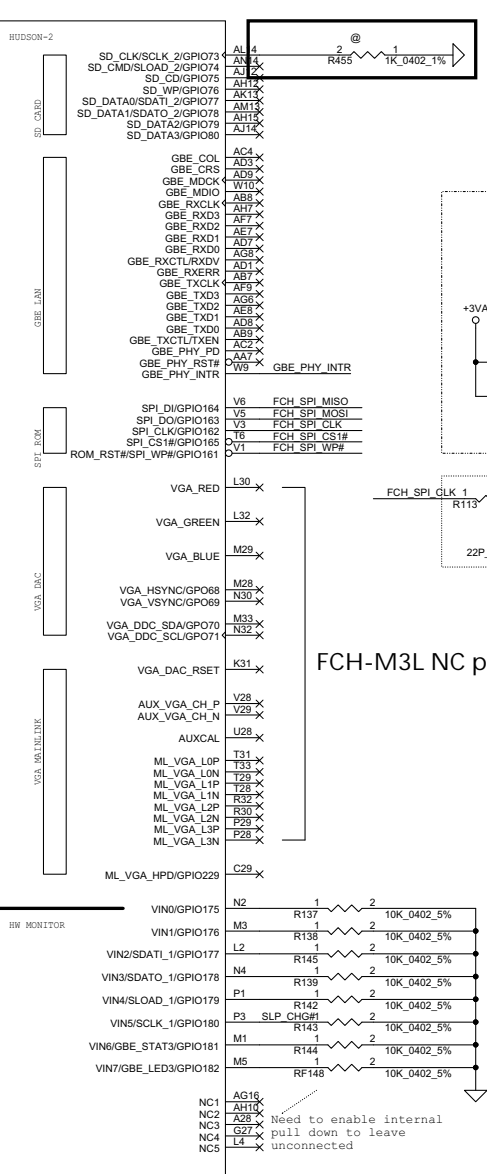
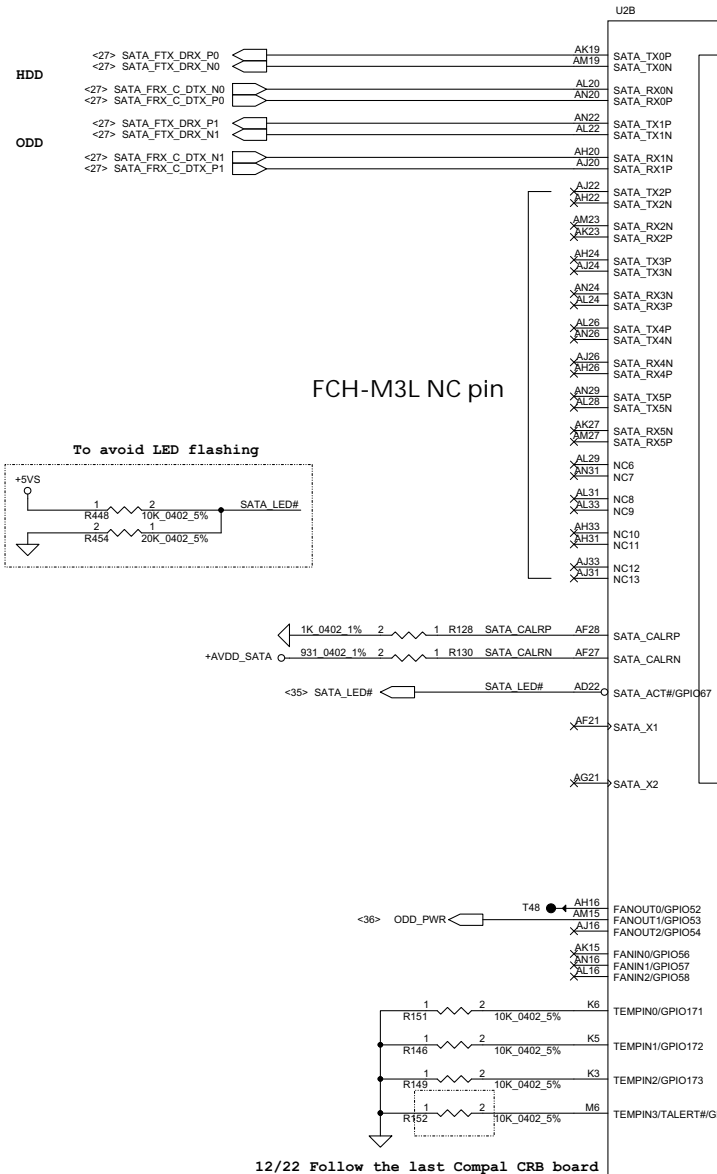
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If use GCLK, please delete D14

DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.

4/23 Change R271 and add R277,R268,C305,+RTCBATT_D



218-0755091 A13 HUDSON-M3L FCBGA 656P C38

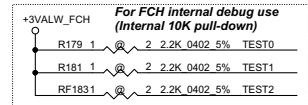
M3LR1@

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				4019K4		
				Date:	Saturday, September 07, 2013	Sheet 23 of 47

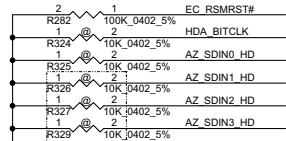
PCIE_RST2 : Reset PCIE device on Hudson 3

U2D

HUDSON-2

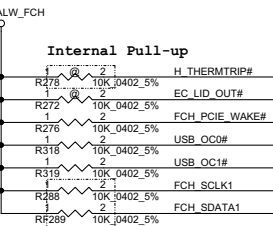


SM Bus 0-->S0 PWR domain==> SO-DIMM, WLAN
SM Bus 1-->S5 PWR domain==> no use

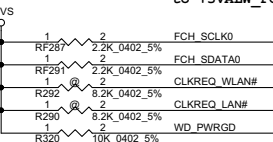


12/22 Reserve R326,R327,R329 but AMD have internal pull down

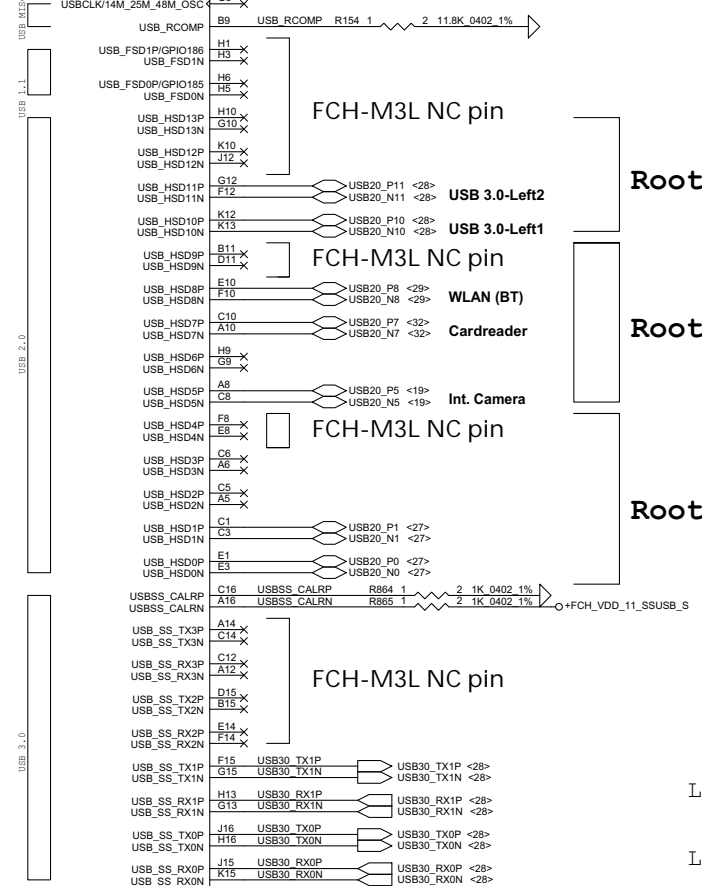
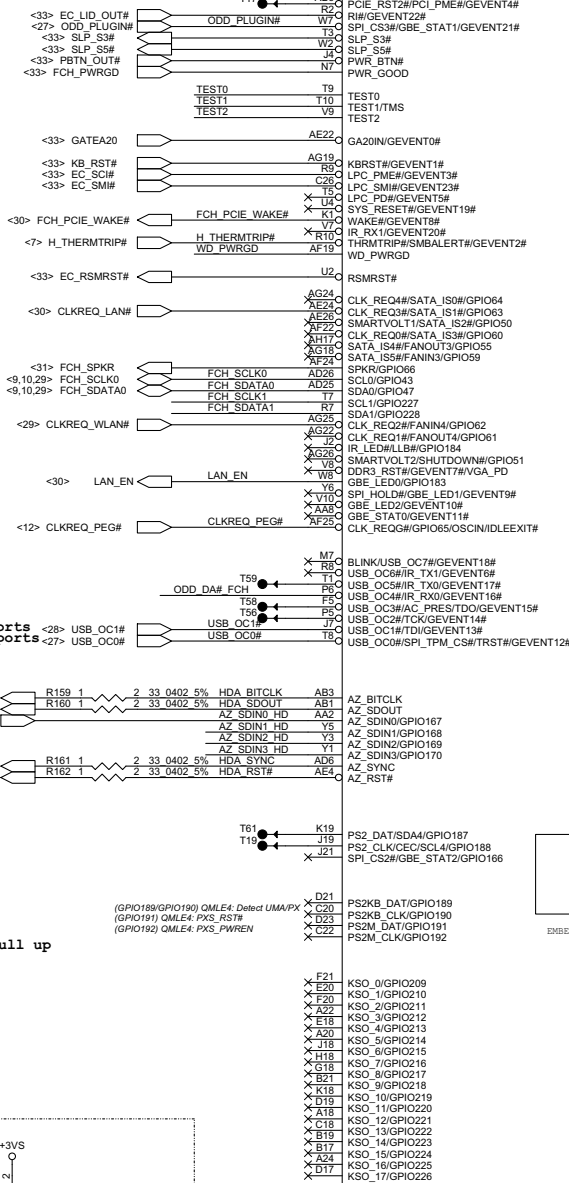
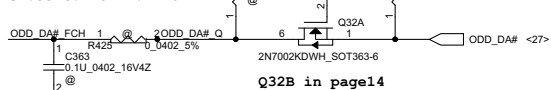
USB_OC1# is for left USB3.0 ports
USB_OC0# is for right USB2.0 ports



12/22 SMBus Not Implemented use 10k pull up to +3VALW_FCH



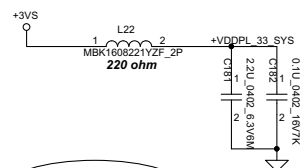
Place R425 and C363 close to FCH for ESD



218-0755091 A13 HUDSON-M3L FCBGA 656P C38

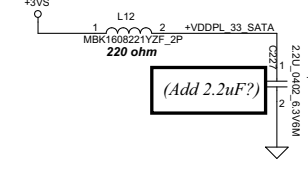
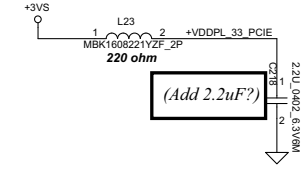
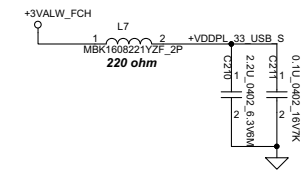
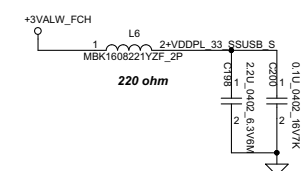
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Date: Saturday, September 07, 2013				Rev B
Sheet 24 of 47				



del +VDDPL_33_MLDAC power plane

del +FCH_VDDAN_33_DAC power plane

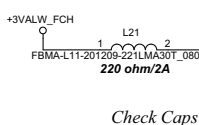


VDDPL_33_SSUSB_S
For Hudson3 USB3.0 only
For Hudson2, connect to GND

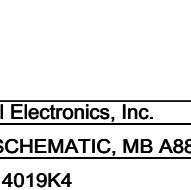
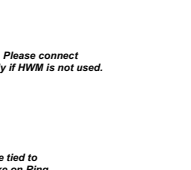
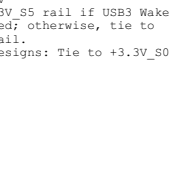
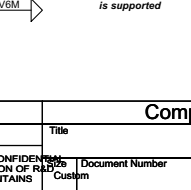
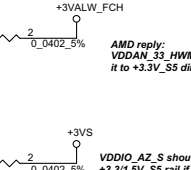
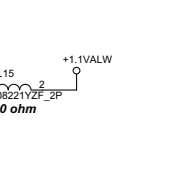
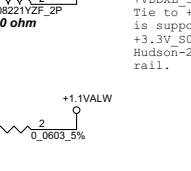
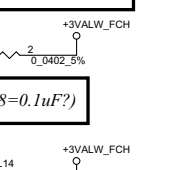
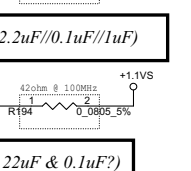
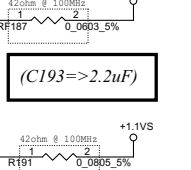
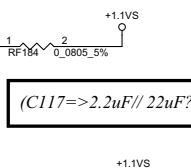
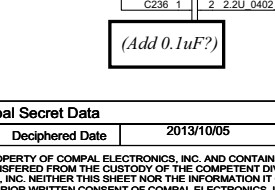
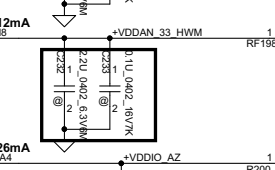
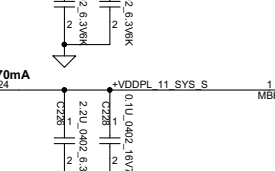
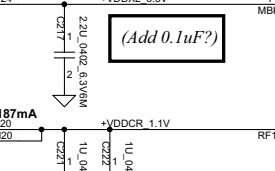
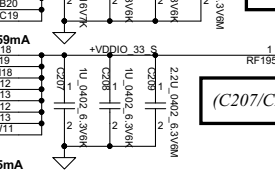
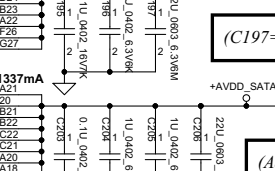
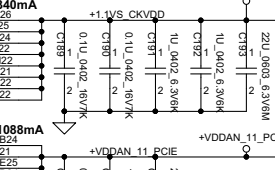
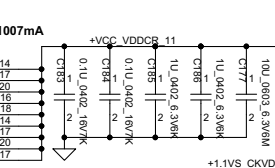
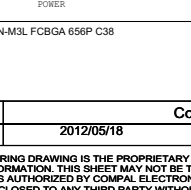
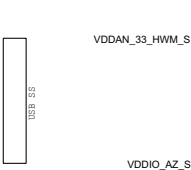
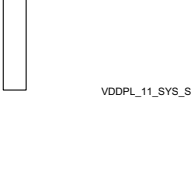
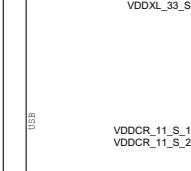
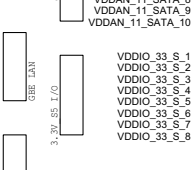
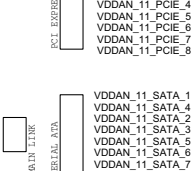
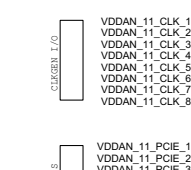
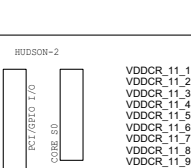
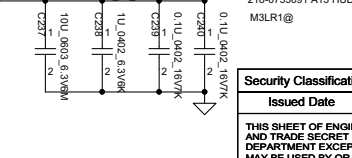
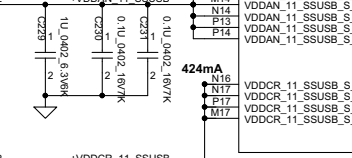
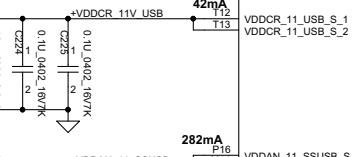
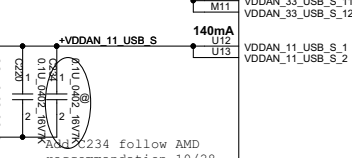
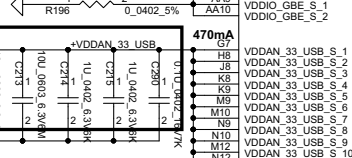
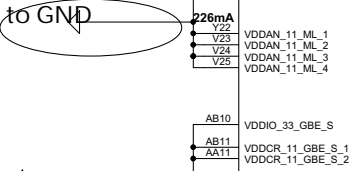
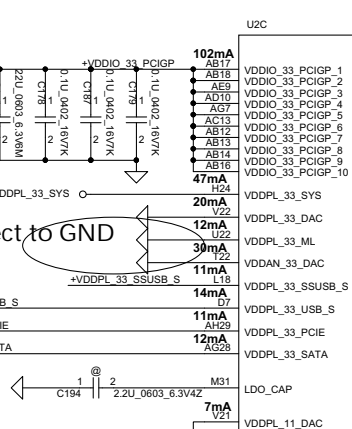
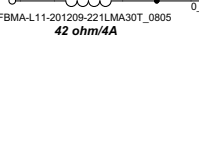
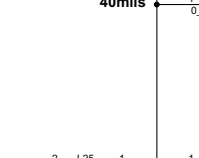
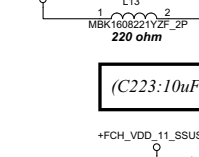
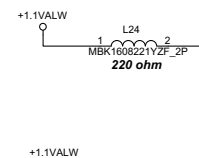
LDO_CAP: Internally generated 1.8V
supply for the RGB outputs

demo board connect to GND

demo board connect to GND



Check Caps



218-0755091 A13 HUDSON-M3L FCBGA 656P C38

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				Customer	Rev B
				Date:	Saturday, September 07, 2013
				Sheet	25 of 47

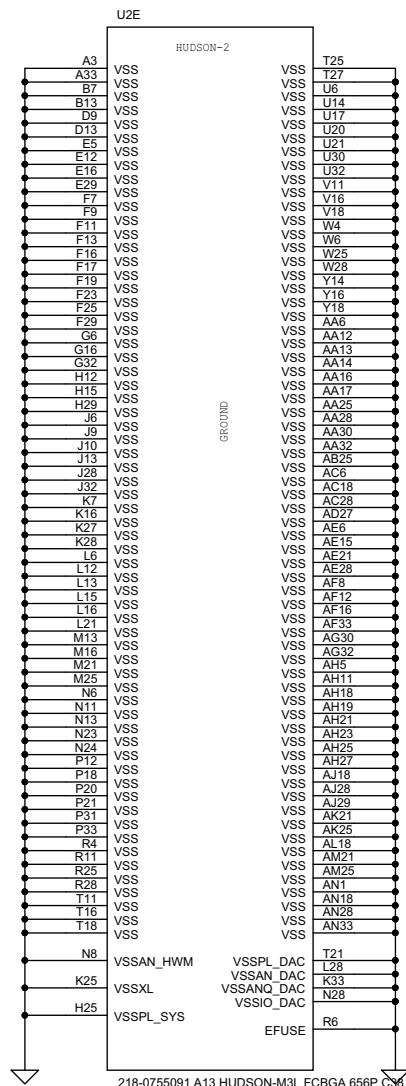
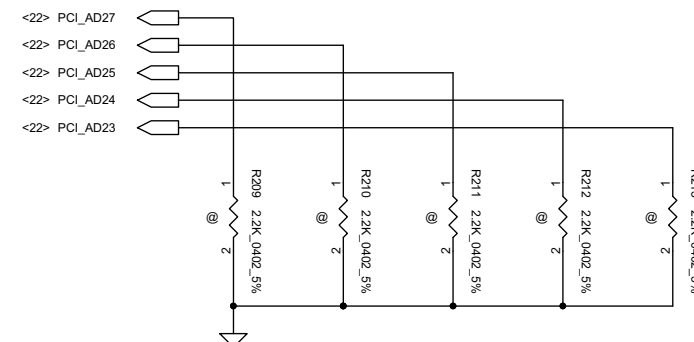
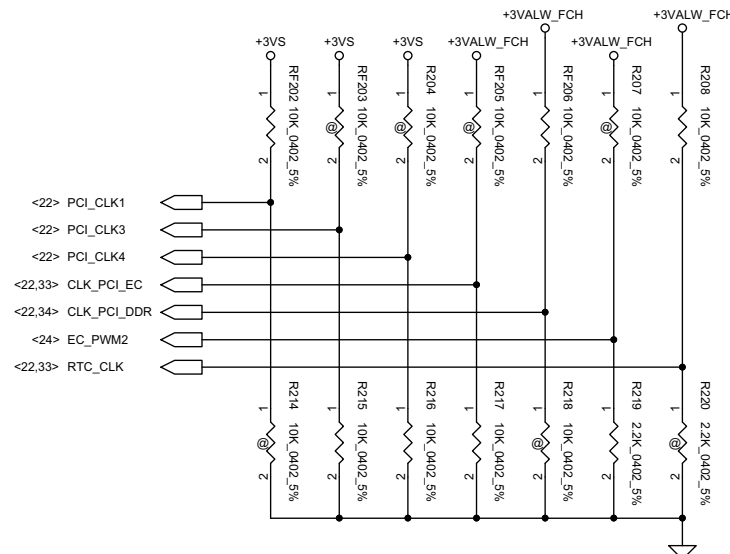
STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

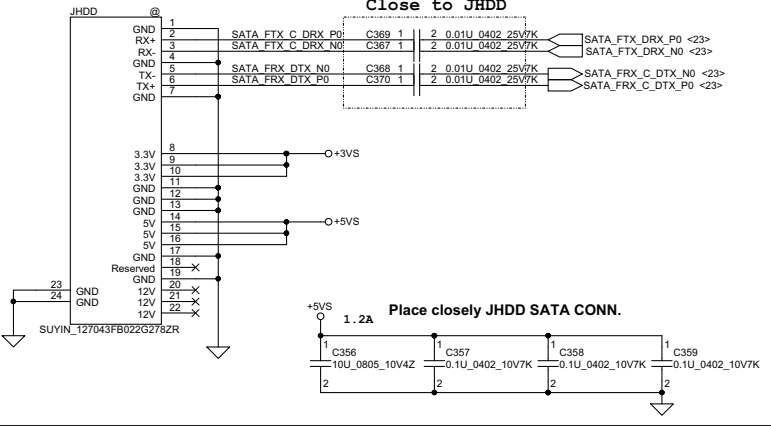
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

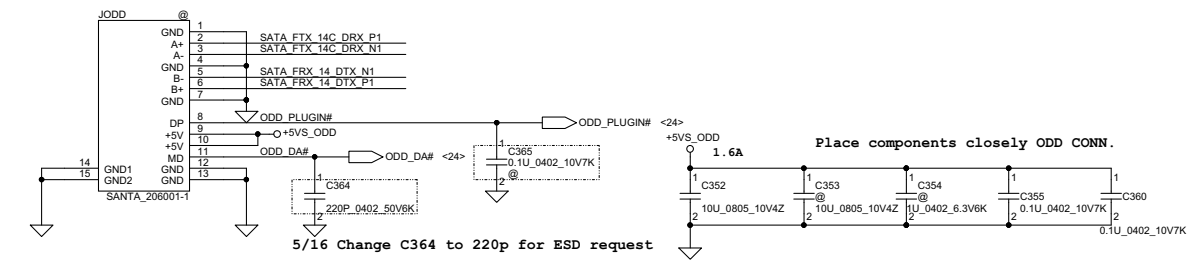


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				4019K4		
				Date:	Saturday, September 07, 2013	Sheet 26 of 47

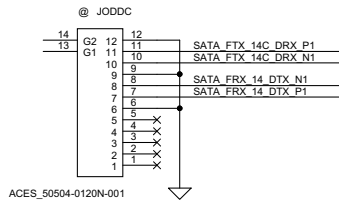
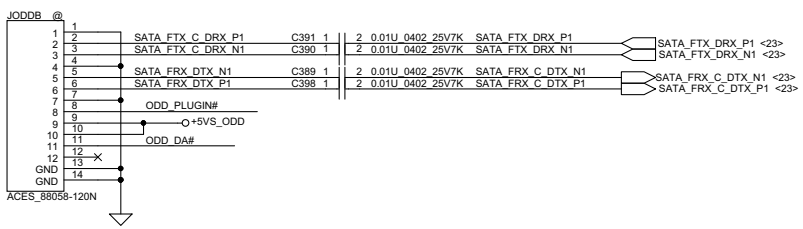
SATA HDD Conn.



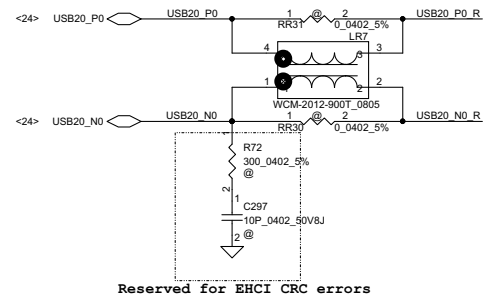
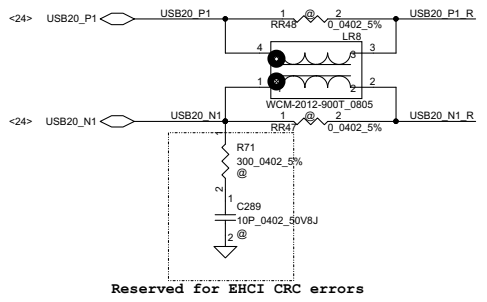
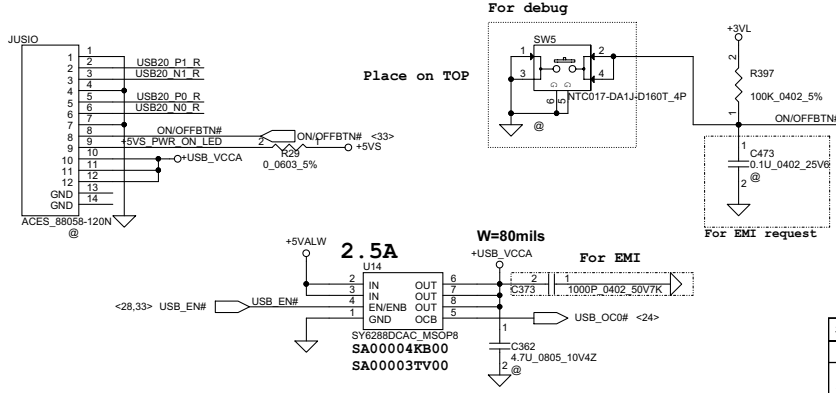
SATA ODD Conn (for 14")



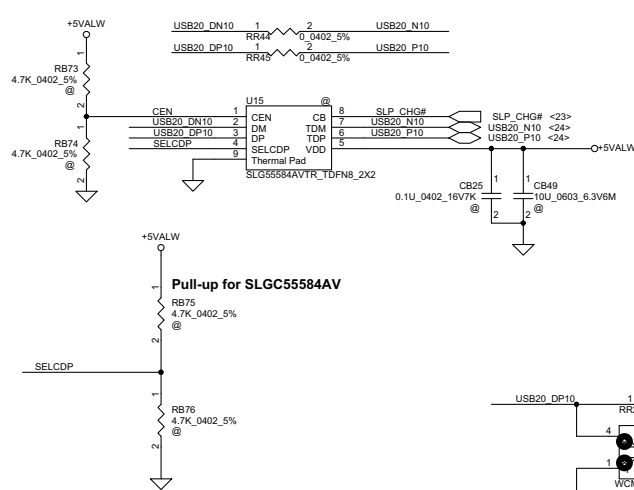
SATA ODD Conn (for 15")



Power Button & RUSB connector

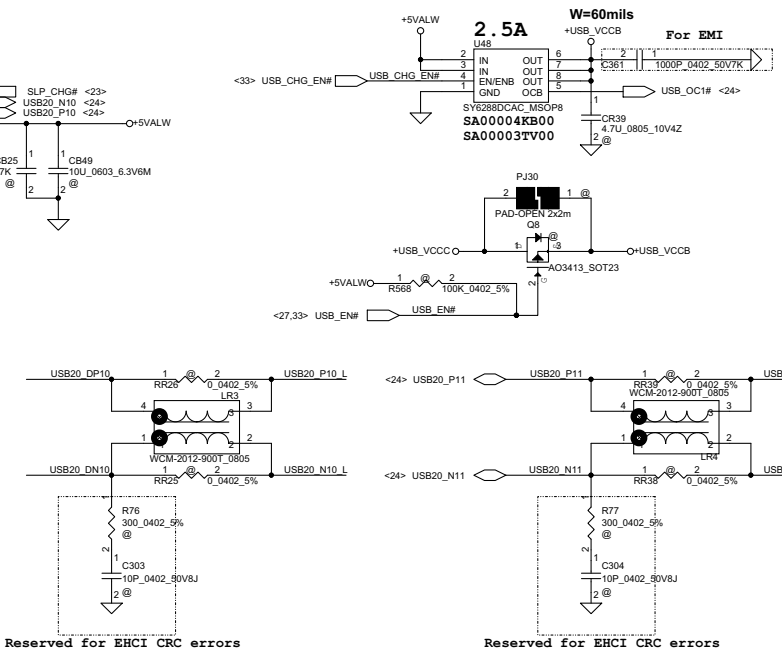


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4019K4				Sheet 27 of 47



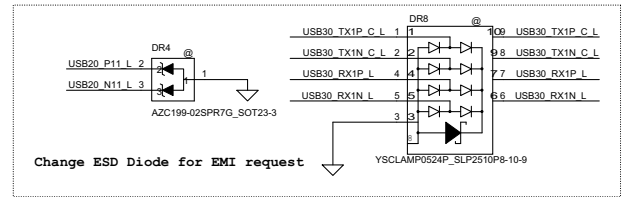
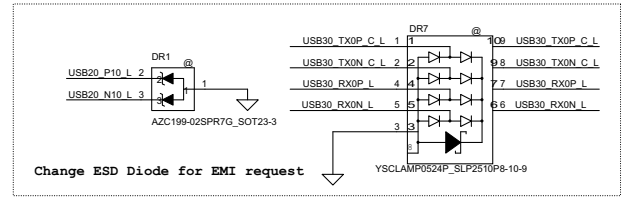
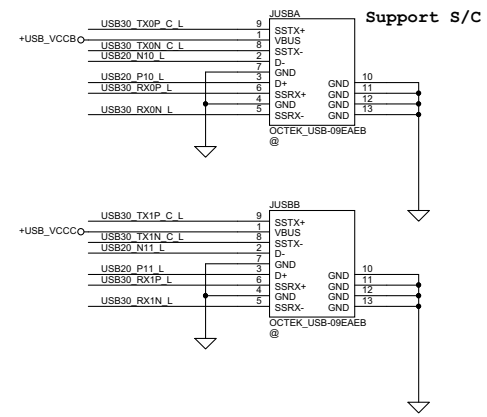
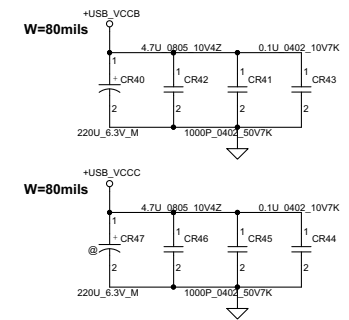
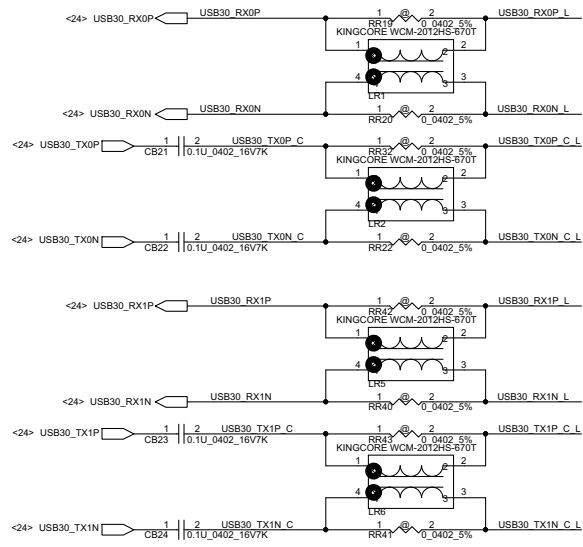
Pull-up for SLC5584AV

SLP_CHG#	SELCDP	Function
0	X	DCP autotdetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only

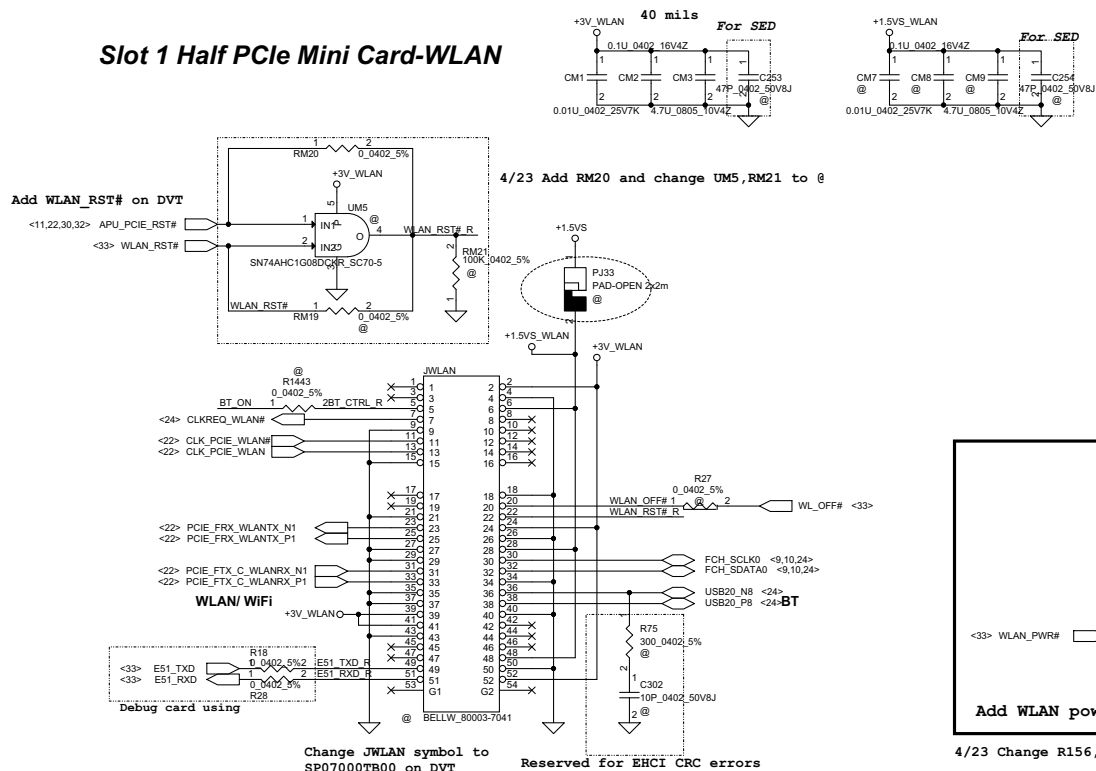


Reserved for EHCI CRC errors


Reserved for EHCI CRC errors



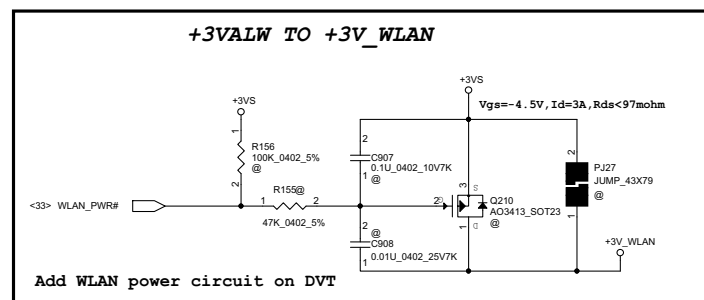
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		Date	Saturday, September 07, 2013
		Sheet	28 of 47

Slot 1 Half PCIe Mini Card-WLANWLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT ON	H	L

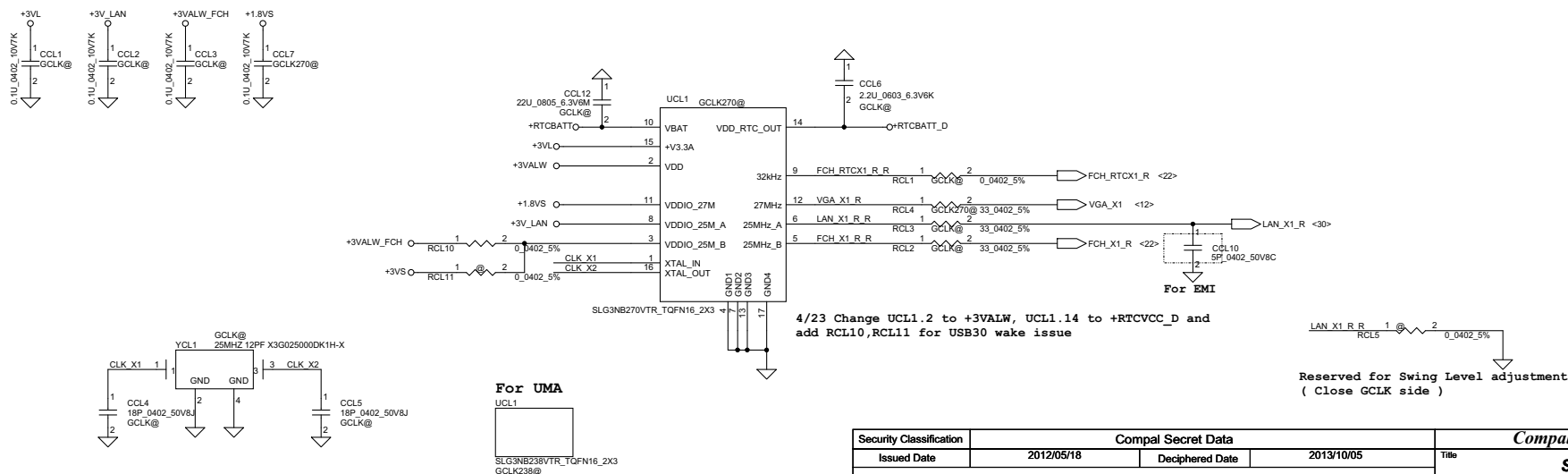
<33> BT_ON  1 R328 2 E51 RXD R
1K_0402 5%

For isolate BT_CTRL and
Compal Debug Card.

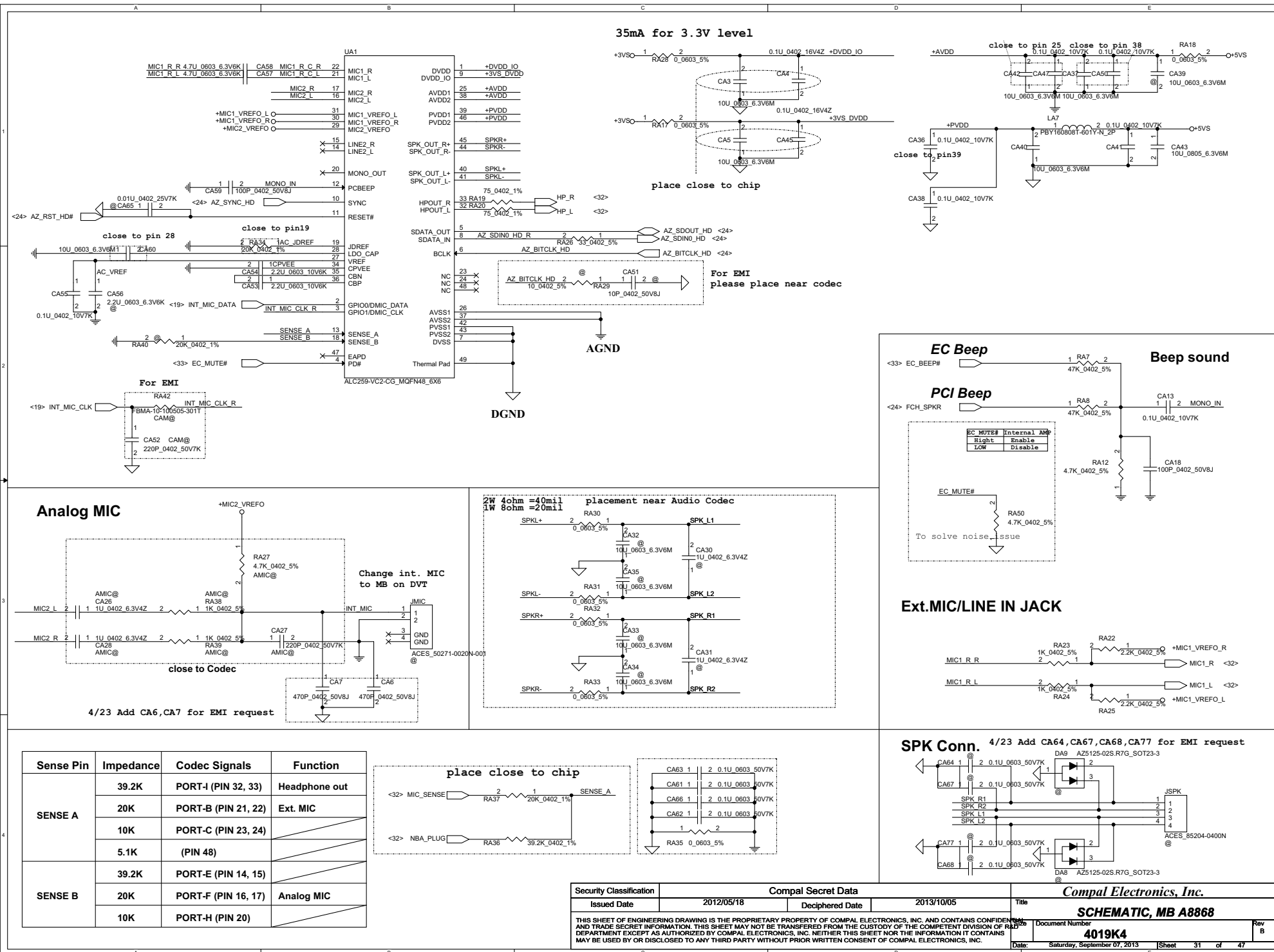


4/23 Change R156,R155,C907,C908,Q210 to e

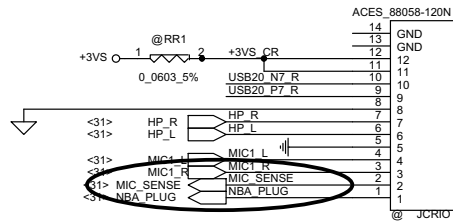
Green Clock Generator



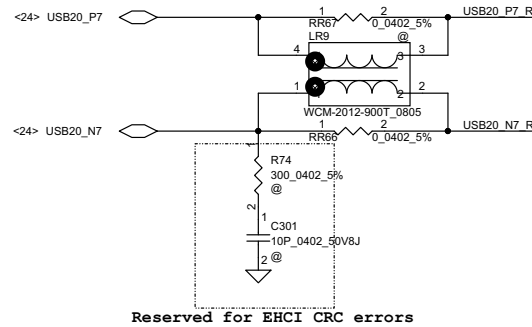
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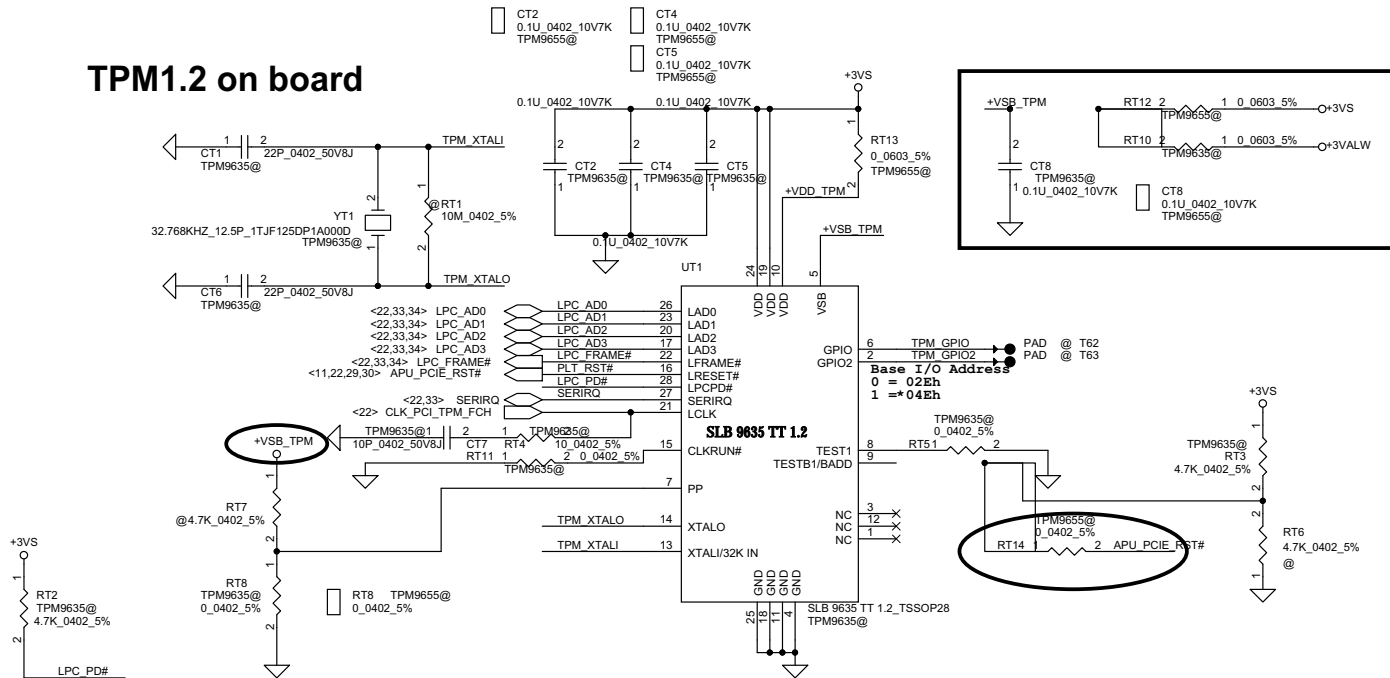
CardReader Conn.



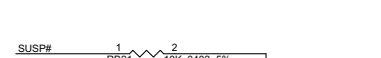
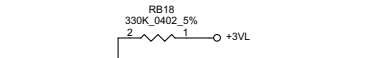
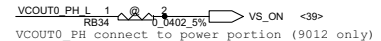
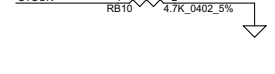
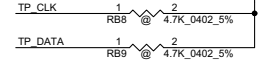
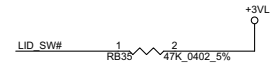
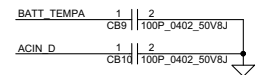
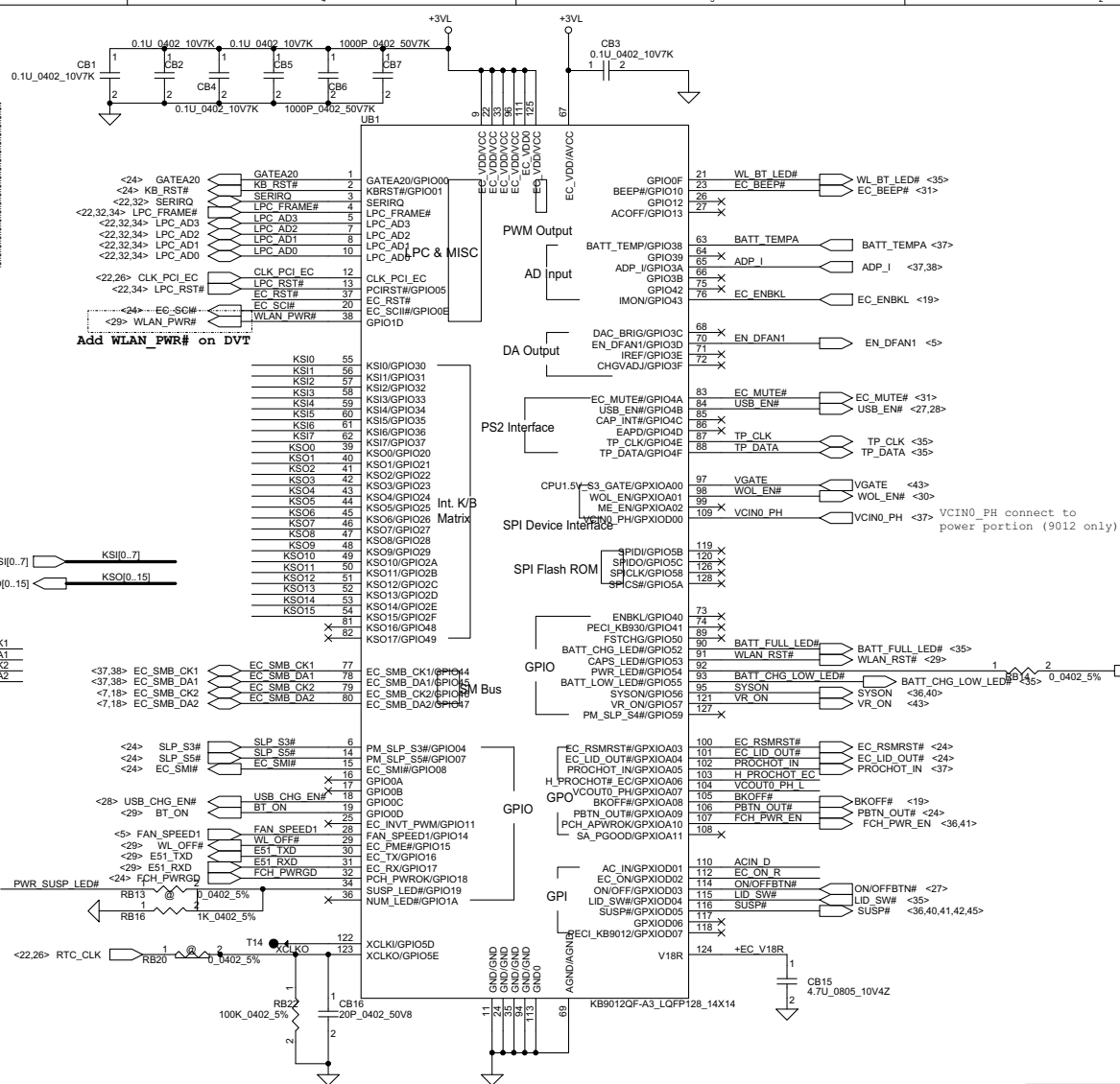
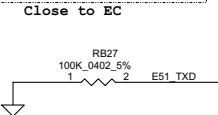
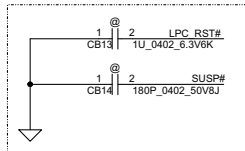
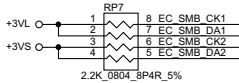
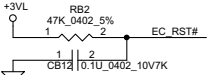
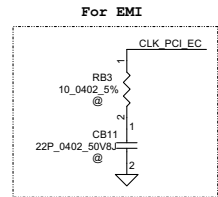
Update JCRI0 pin definition on DVT



TPM1.2 on board

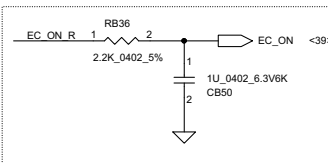


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				Date:	Saturday, September 07, 2013
				Sheet	32 of 47

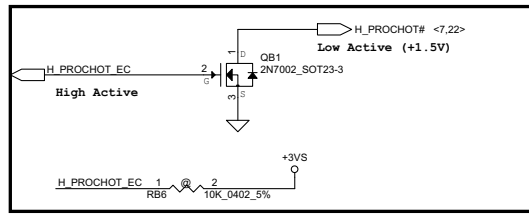


Voltage Comparator Pins FOR 9012 A3

VCIN0 pin109	>1.2V	<1.2V
VCIN1 pin102		
VCOUT0 pin104	HIGH	LOW
VCOUT1 pin103	LOW	HIGH



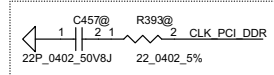
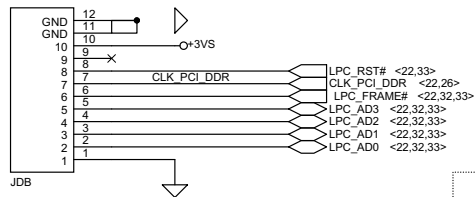
For KB9012 EC ON low pulse work around



LPC Debug Port

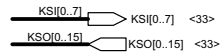
Place the PAD under DDR DIMM.

@
E-T_3801K-F10N-01L

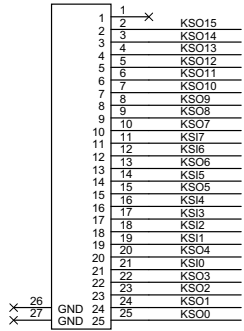


For EMI

KEYBOARD CONN.



JKB



ACES_50524-02501-001
@

For EMI

Close to JKB

KSO2	1	2
C404	1	100P_0402_50V8J
KSO1	1	2
C405	1	100P_0402_50V8J
KSO0	1	2
C406	1	100P_0402_50V8J
KSO4	1	2
C407	1	100P_0402_50V8J
KSO3	1	2
C408	1	100P_0402_50V8J
KSO5	1	2
C409	1	100P_0402_50V8J
KSO14	1	2
C410	1	100P_0402_50V8J
KSO6	1	2
C411	1	100P_0402_50V8J
KSO7	1	2
C412	1	100P_0402_50V8J
KSO13	1	2
C413	1	100P_0402_50V8J
KSO8	1	2
C415	1	100P_0402_50V8J
KSO9	1	2
C416	1	100P_0402_50V8J
KSO10	1	2
C417	1	100P_0402_50V8J
KSO11	1	2
C418	1	100P_0402_50V8J
KSO12	1	2
C419	1	100P_0402_50V8J
KSO15	1	2
C420	1	100P_0402_50V8J
KSI7	1	2
C421	1	100P_0402_50V8J
KSI2	1	2
C422	1	100P_0402_50V8J
KSI3	1	2
C423	1	100P_0402_50V8J
KSI4	1	2
C424	1	100P_0402_50V8J
KSI0	1	2
C425	1	100P_0402_50V8J
KSI5	1	2
C427	1	100P_0402_50V8J
KSI6	1	2
C429	1	100P_0402_50V8J
KSI1	1	2
C431	1	100P_0402_50V8J

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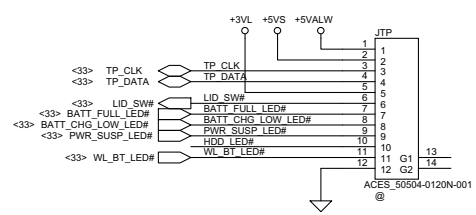
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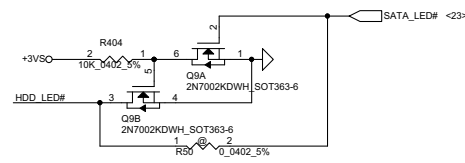
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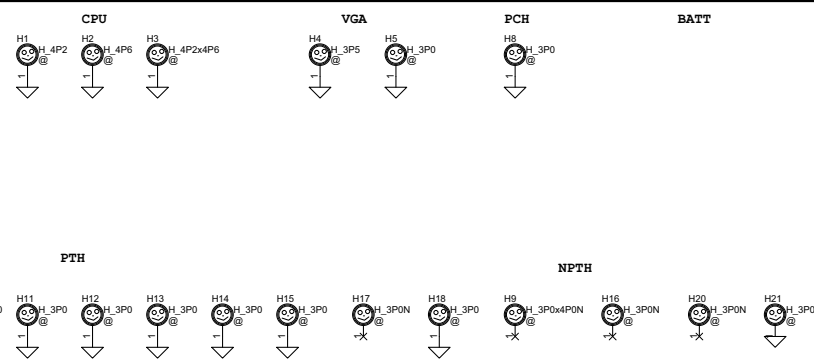
Touchpad Connector
(Reserve 7 pins for LED & Win8 TP)



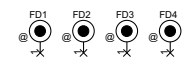
HDD LED



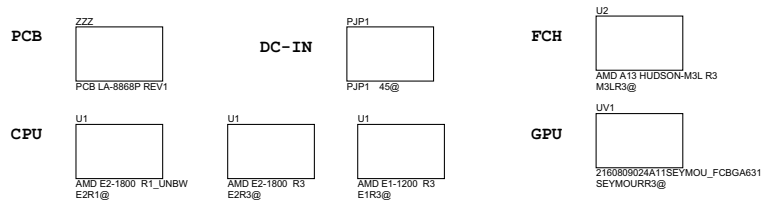
Screw Hole



PCB Federal Mark PAD

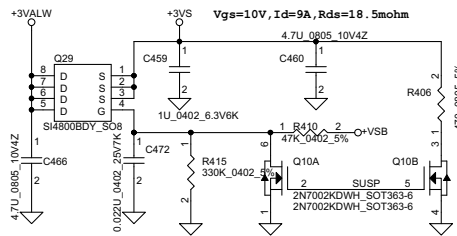


ISPD

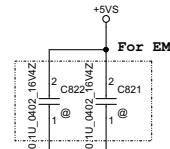
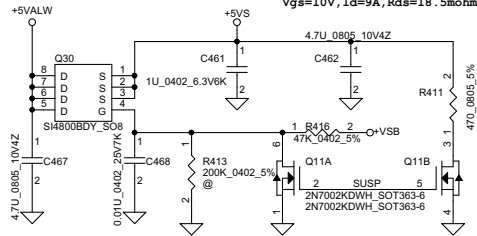


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				4019K4	Rev B
				Date	Sheet
				Saturday, September 07, 2013	35 of 47

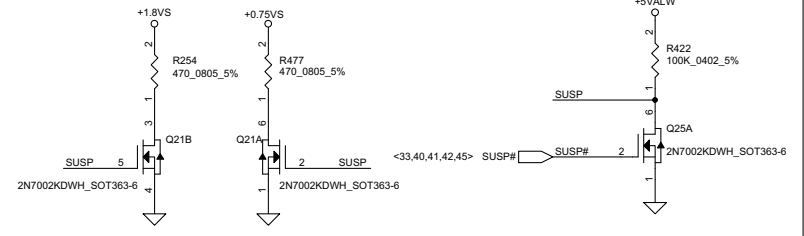
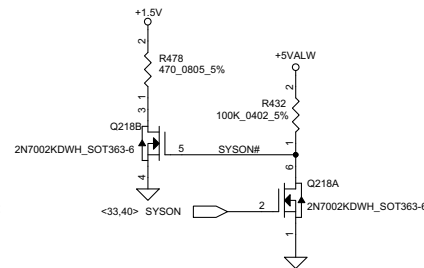
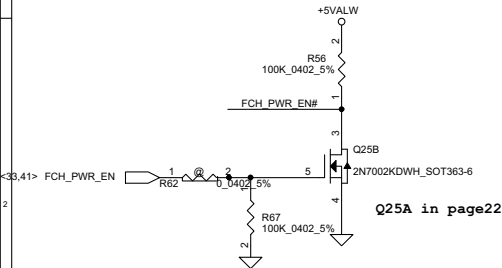
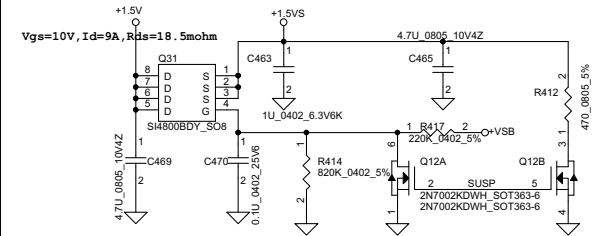
+3VALW TO +3VS



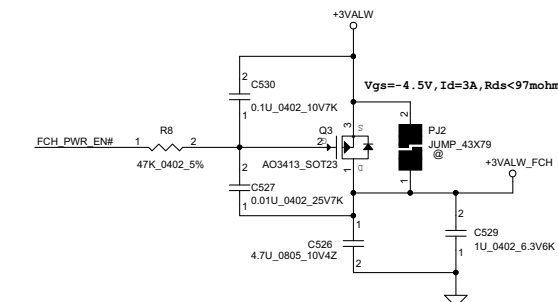
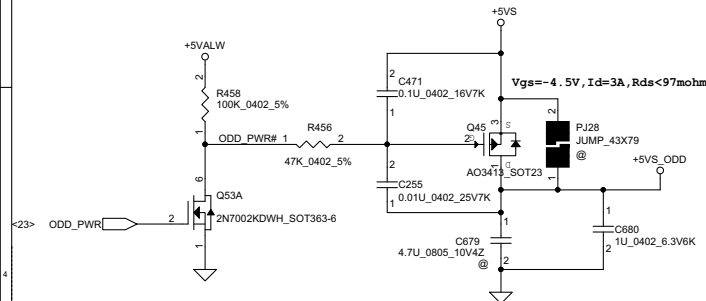
+5VALW TO +5VS



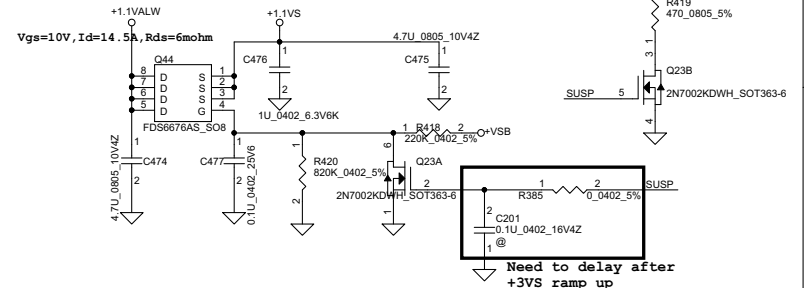
+1.5V to +1.5VS



+5VS TO +5VS_ODD



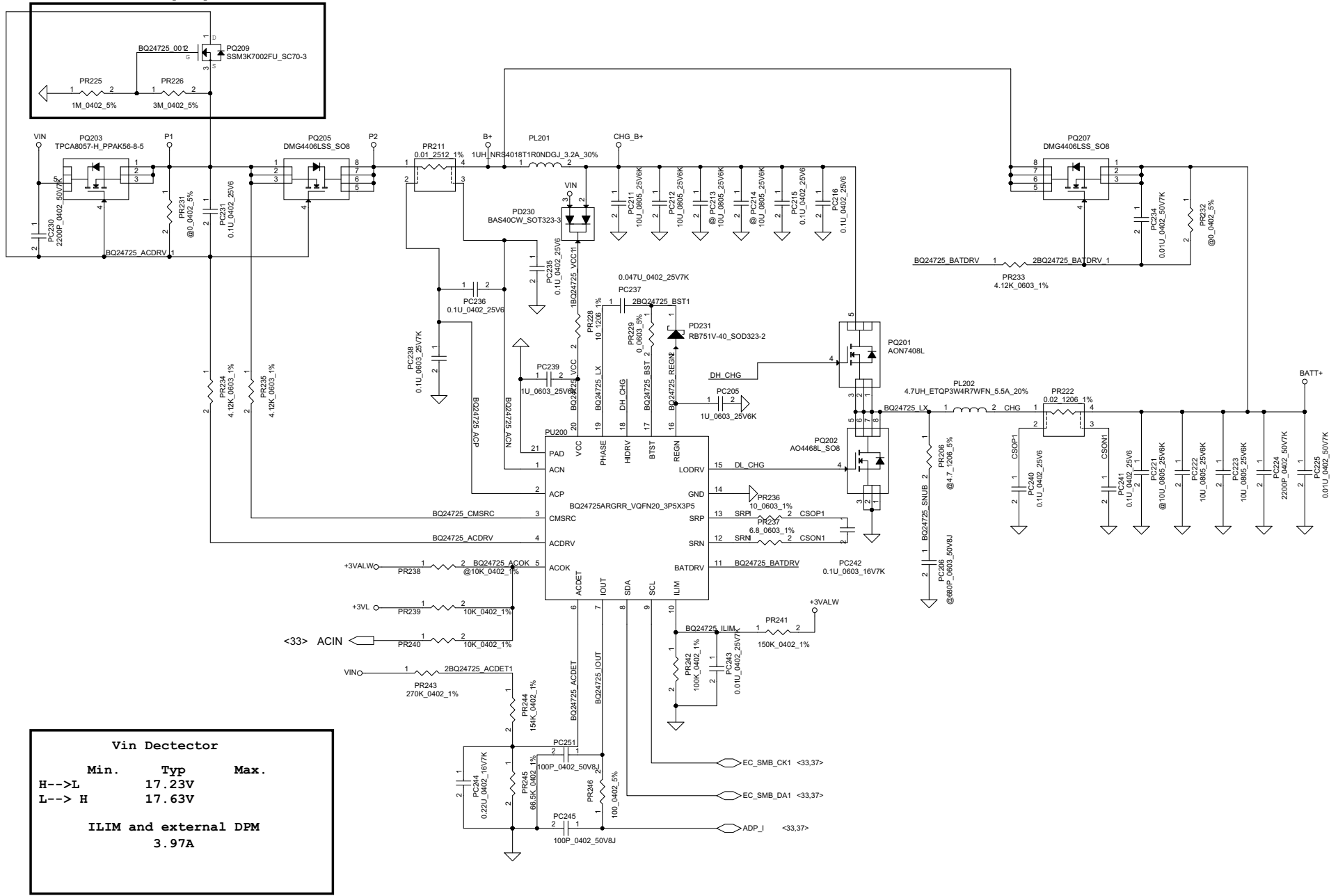
+1.1VALW to +1.1VS

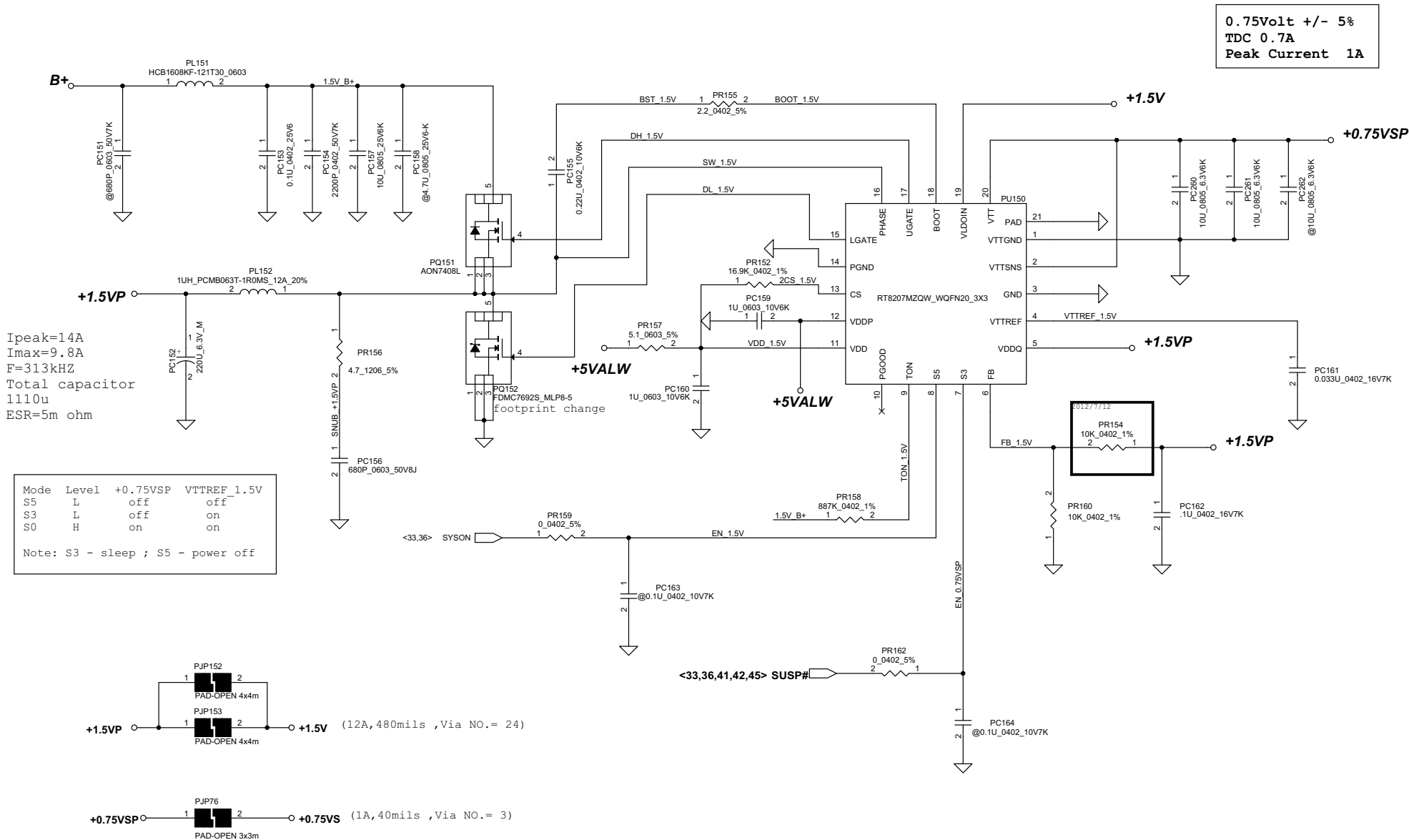


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Date: Saturday, September 07, 2013			Sheet 36	of 47

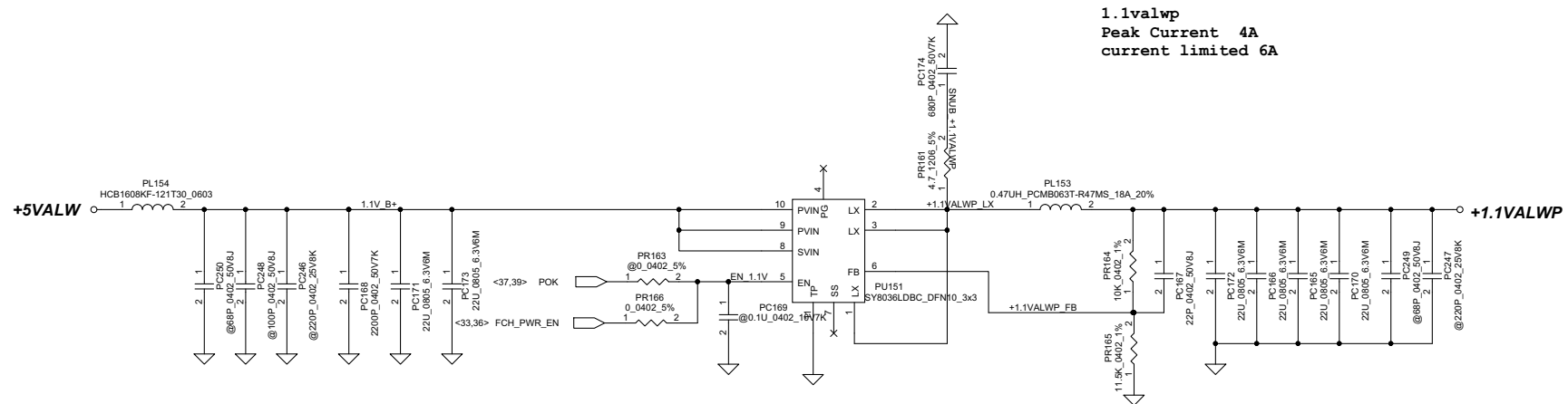
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for reverse input protection

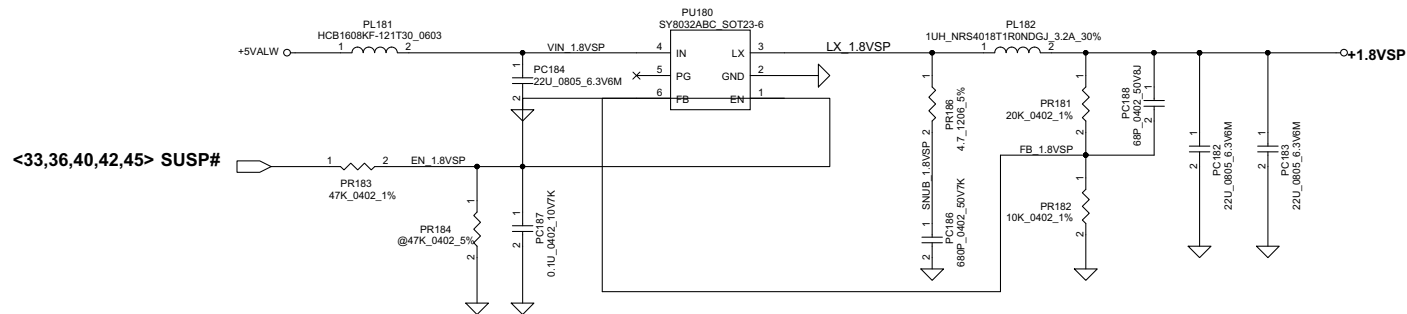





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				Date	Saturday, September 07, 2013
				Sheet	40 of 47



+1.1VALWP  +1.1VALW (4A,240mils ,Via NO.= 8)
PAD-OPEN 4x4mm



+1.8VSP  +1.8VS (3A,120mils ,Via NO.= 6)
PAD-OPEN 4x4mm

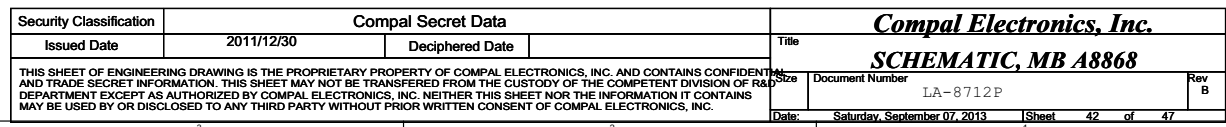
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				LA-8712P	B
				Date: Saturday, September 07, 2013	Sheet 41 of 47

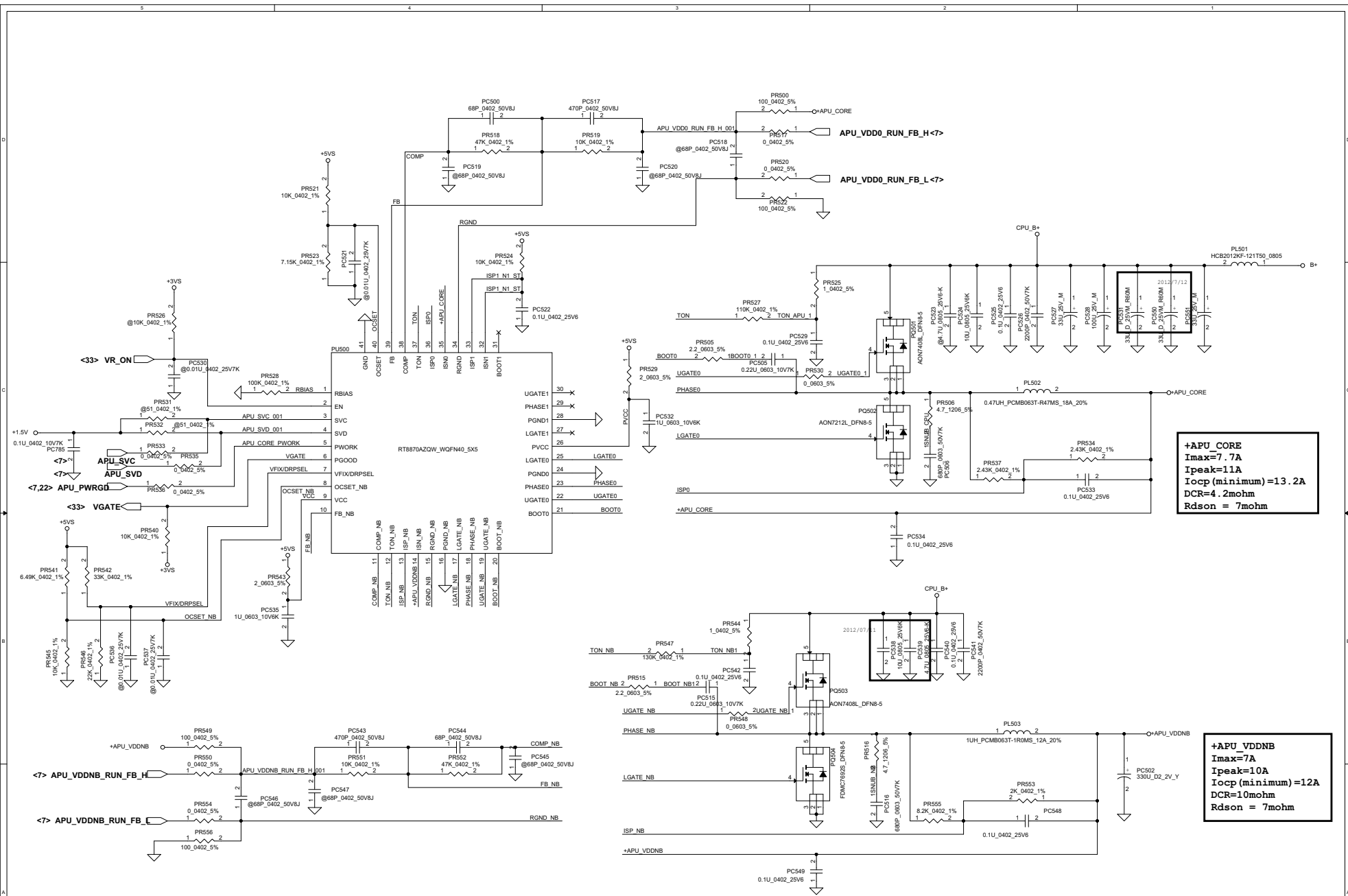
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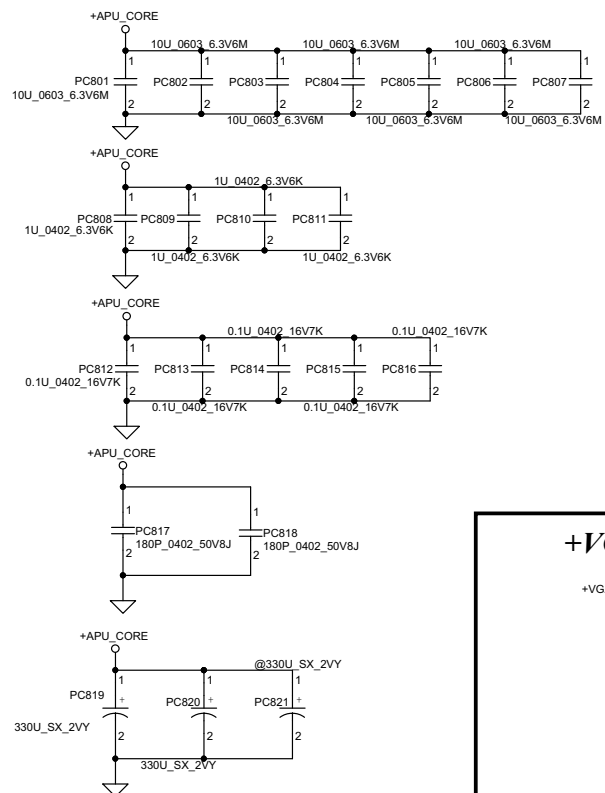
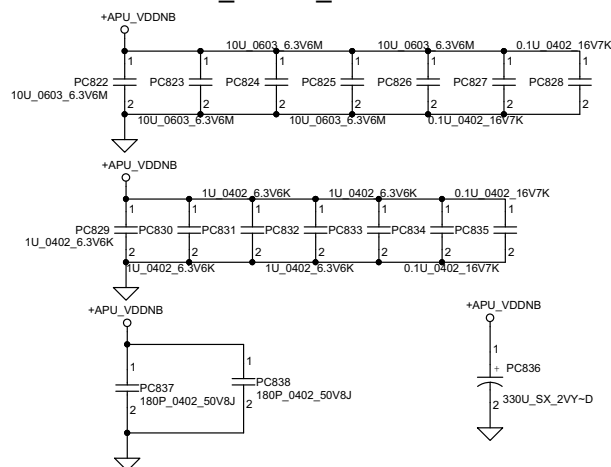
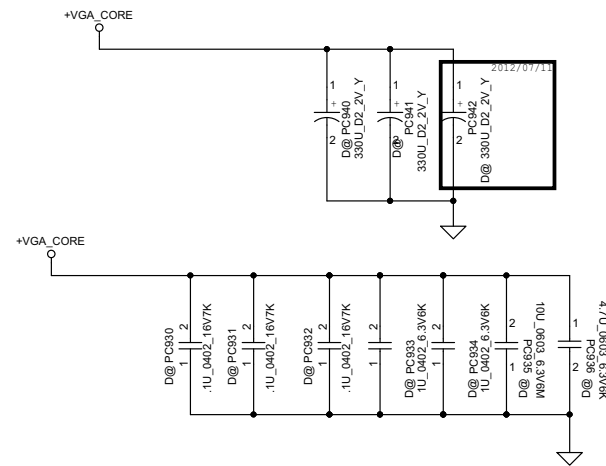
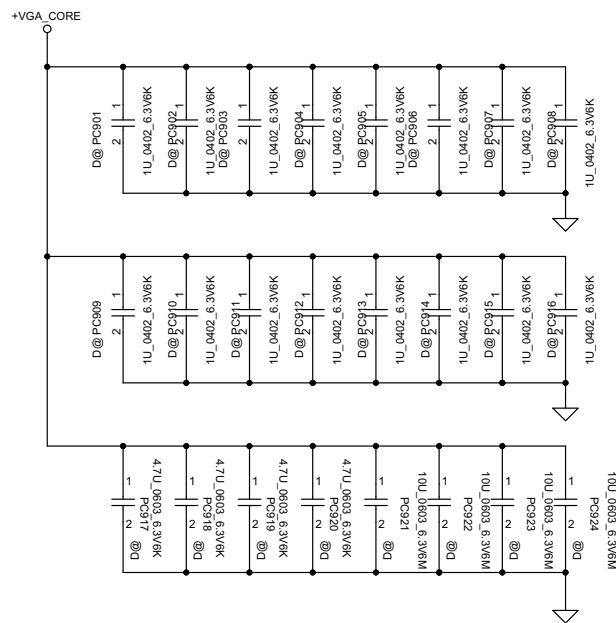
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Date: Saturday, September 07, 2013 Sheet 41 of 47





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			Document Number 4019K4
			Date Saturday, September 07, 2013 15:00:43 of 47

+*APU_CORE*+*APU_CORE_NB*+*VGA_CORE*

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				Size	Document Number		Rev	
				A3	LA-8712P		B	
Date:				Saturday, September 07, 2013	Sheet	44	of 47	

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